

ENGINEERING MATHEMATICS – III

Sub Code	: 10MAT31	IA Marks	: 25
Hrs/ Week	: 04	Exam Hours	: 03
Total Hrs.	: 52	Exam Marks	: 100

PART-A

UNIT-1

Fourier series

Convergence and divergence of infinite series of positive terms, definition and illustrative examples*

Periodic functions, Dirichlet's conditions, Fourier series of periodic functions of period 2π and arbitrary period, half range Fourier series. Complex form of Fourier Series. Practical harmonic analysis.

7 Hours

UNIT-2

Fourier Transforms

Infinite Fourier transform, Fourier Sine and Cosine transforms, properties, Inverse transforms

6 Hours

UNIT-3

Application of PDE

Various possible solutions of one dimensional wave and heat equations, two dimensional Laplace's equation by the method of separation of variables, Solution of all these equations with specified boundary conditions. D'Alembert's solution of one dimensional wave equation.

6 Hours

UNIT-4

Curve Fitting and Optimisation

Curve fitting by the method of least squares- Fitting of curves of the form

$$y = ax + b, \quad y = ax^2 + bx + c, \quad y = ae^{bx}, \quad y = ax^b$$

Optimization: Linear programming, mathematical formulation of linear programming problem (LPP), Graphical method and simplex method.

7 Hours

PART-B

UNIT-5

Numerical Methods - 1

Numerical Solution of algebraic and transcendental equations: Regula-falsi method, Newton - Raphson method. Iterative methods of solution of a system

of equations: Gauss-seidel and Relaxation methods. Largest eigen value and the corresponding eigen vector by Rayleigh's power method.

6 Hours

UNIT-6

Numerical Methods – 2

Finite differences: Forward and backward differences, Newton's forward and backward interpolation formulae. Divided differences - Newton's divided difference formula, Lagrange's interpolation formula and inverse interpolation formula.

Numerical integration: Simpson's one-third, three-eighth and Weddle's rules (All formulae/rules without proof)

7 Hours

UNIT-7

Numerical Methods – 3

Numerical solutions of PDE – finite difference approximation to derivatives, Numerical solution of two dimensional Laplace's equation, one dimensional heat and wave equations

7 Hours

UNIT-8

Difference Equations and Z-Transforms

Difference equations: Basic definition; Z-transforms – definition, standard Z-transforms, damping rule, shifting rule, initial value and final value theorems. Inverse Z-transform. Application of Z-transforms to solve difference equations.

6 Hours

Note: * In the case of illustrative examples, questions are not to be set.

Text Books:

1. B.S. Grewal, Higher Engineering Mathematics, Latest edition, Khanna Publishers.
2. Erwin Kreyszig, Advanced Engineering Mathematics, Latest edition, Wiley Publications.

Reference Books:

1. B.V. Ramana, Higher Engineering Mathematics, Latest edition, Tata Mc. Graw Hill Publications.
2. Peter V. O'Neil, Engineering Mathematics, CENGAGE Learning India Pvt Ltd. Publishers.

ANALOG ELECTRONIC CIRCUITS
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	: 10ES32	IA Marks	: 25
Hrs/ Week	: 04	Exam Hours	: 03
Total Hrs.	: 52	Exam Marks	: 100

UNIT 1:

Diode Circuits: Diode Resistance, Diode equivalent circuits, Transition and diffusion capacitance, Reverse recovery time, Load line analysis, Rectifiers, Clippers and clampers. **6 Hrs**

UNIT 2:

Transistor Biasing: Operating point, Fixed bias circuits, Emitter stabilized biased circuits, Voltage divider biased, DC bias with voltage feedback, Miscellaneous bias configurations, Design operations, Transistor switching networks, PNP transistors, Bias stabilization. **6 Hrs**

UNIT 3:

Transistor at Low Frequencies: BJT transistor modeling, CE Fixed bias configuration, Voltage divider bias, Emitter follower, CB configuration, Collector feedback configuration, Analysis of circuits r_e model; analysis of CE configuration using h- parameter model; Relationship between h- parameter model of CE, CC and CE configuration. **7 Hrs**

UNIT 4:

Transistor Frequency Response: General frequency considerations, low frequency response, Miller effect capacitance, High frequency response, multistage frequency effects. **7 Hrs**

UNIT 5:

(a) General Amplifiers: Cascade connections, Cascode connections, Darlington connections. **3 Hrs**

(b) Feedback Amplifier: Feedback concept, Feedback connections type, Practical feedback circuits. Design procedures for the feedback amplifiers. **4 Hrs**

UNIT 6:

Power Amplifiers: Definitions and amplifier types, series fed class A amplifier, Transformer coupled Class A amplifiers, Class B amplifier operations, Class B amplifier circuits, Amplifier distortions. Designing of Power amplifiers. **7 Hrs**

UNIT 7:

Oscillators: Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (BJT Version Only) Simple design methods of Oscillators. **6 Hrs**

UNIT 8:

FET Amplifiers: FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks. **6 Hrs**

TEXT BOOK:

1. **“Electronic Devices and Circuit Theory”**, Robert L. Boylestad and Louis Nashelsky, PHI/Pearson Education. 9TH Edition.

REFERENCE BOOKS:

1. **“Integrated Electronics”**, Jacob Millman & Christos C. Halkias, Tata - McGraw Hill, 2nd Edition, 2010
2. **“Electronic Devices and Circuits”**, David A. Bell, PHI, 4th Edition, 2004
3. **“Analog Electronics Circuits: A Simplified Approach”**, U.B. Mahadevaswamy, Pearson/Saguine, 2007.

LOGIC DESIGN
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	10ES33	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

UNIT 1:

Principles of combinational logic-1: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-3, 4 and 5 variables, Incompletely specified functions (Don't Care terms), Simplifying Max term equations. **6 Hrs**

UNIT 2:

Principles of combinational Logic-2: Quine-McCluskey minimization technique- Quine-McCluskey using don't care terms, Reduced Prime Implicant Tables, Map entered variables. **7 Hrs**

UNIT 3:

Analysis and design of combinational logic - I: General approach, Decoders-BCD decoders, Encoders. **6 Hrs**

UNIT 4:

Analysis and design of combinational logic - II: Digital multiplexers- Using multiplexers as Boolean function generators. Adders and subtractors- Cascading full adders, Look ahead carry, Binary comparators. Design methods of building blocks of combinational logics. **7 Hrs**

UNIT 5:

Sequential Circuits – 1: Basic Bistable Element, Latches, SR Latch, Application of SR Latch, A Switch Debouncer, The \bar{S} \bar{R} Latch, The gated SR Latch, The gated D Latch, The Master-Slave Flip-Flops (Pulse-Triggered Flip-Flops): The Master-Slave SR Flip-Flops, The Master-Slave JK Flip-Flop, Edge Triggered Flip-Flop: The Positive Edge-Triggered D Flip-Flop, Negative-Edge Triggered D Flip-Flop. **7 Hrs**

UNIT 6:

Sequential Circuits – 2: Characteristic Equations, Registers, Counters - Binary Ripple Counters, Synchronous Binary counters, Counters based on Shift Registers, Design of a Synchronous counters, Design of a Synchronous Mod-6 Counter using clocked JK Flip-Flops Design of a Synchronous Mod-6 Counter using clocked D, T, or SR Flip-Flops **7 Hrs**

UNIT 7:

Sequential Design - I: Introduction, Mealy and Moore Models, State Machine Notation, Synchronous Sequential Circuit Analysis and Design. **6 Hrs**

UNIT 8:

Sequential Design - II: Construction of state Diagrams, Counter Design. **6 Hrs**

TEXT BOOKS:

1. “**Digital Logic Applications and Design**”, John M Yarbrough, Thomson Learning, 2001.
2. “**Digital Principles and Design** “, Donald D Givone, Tata McGraw Hill Edition, 2002.

REFERENCE BOOKS:

1. “**Fundamentals of logic design**”, Charles H Roth, Jr; Thomson Learning, 2004.
2. “**Logic and computer design Fundamentals**”, Mono and Kim, Pearson, Second edition, 2001.
3. “**Logic Design**”, Sudhakar Samuel, Pearson/Saguine, 2007

NETWORK ANALYSIS
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	10ES34	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

UNIT 1:

Basic Concepts: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis With linearly dependent and independent sources for DC and AC networks, Concepts of super node and super mesh. **7 Hrs**

UNIT 2:

Network Topology: Graph of a network, Concept of tree and co-tree, incidence matrix, tie-set, tie-set and cut-set schedules, Formulation of equilibrium equations in matrix form, Solution of resistive networks, Principle of duality. **7 Hrs**

UNIT 3:

Network Theorems – 1: Superposition, Reciprocity and Millman’s theorems. **6 Hrs**

UNIT 4:

Network Theorems - II:

Thevinin’s and Norton’s theorems; Maximum Power transfer theorem
.
6 Hrs

UNIT 5: Resonant Circuits: Series and parallel resonance, frequency-response of series and Parallel circuits, Q –factor, Bandwidth.
7 Hrs

UNIT 6:
Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.
7 Hrs

UNIT 7:
Laplace Transformation & Applications : Solution of networks, step, ramp and impulse responses, waveform Synthesis.
6 Hrs

UNIT 8:
Two port network parameters: Definition of z, y, h and transmission parameters, modeling with these parameters, relationship between parameters sets.
6 Hrs

TEXT BOOKS:

1. “**Network Analysis**”, M. E. Van Valkenburg, PHI / Pearson Education, 3rd Edition. Reprint 2002.
2. “**Networks and systems**”, Roy Choudhury, 2nd edition, 2006 re-print, New Age International Publications.

REFERENCE BOOKS:

1. “**Engineering Circuit Analysis**”, Hayt, Kemmerly and DurbinTMH 7th Edition, 2010
2. “**Basic Engineering Circuit Analysis**”, J. David Irwin / R. Mark Nelms, John Wiley, 8th ed, 2006.
3. “**Fundamentals of Electric Circuits**”, Charles K Alexander and Mathew N O Sadiku, Tata McGraw-Hill, 3 ed, 2009.

ELECTRONIC INSTRUMENTATION
(Common to EC/TC/IT/BM/ML)

Sub Code	:	10IT35	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

UNIT – 1:

Introduction

(a) **Measurement Errors:** Gross errors and systematic errors, Absolute and relative errors, Accuracy, Precision, Resolution and Significant figures.

(b) **Voltmeters and Multimeters** Introduction, Multirange voltmeter, Extending voltmeter ranges, Loading, AC voltmeter using Rectifiers – Half wave and full wave, Peak responding and True RMS voltmeters.

3 + 4 Hrs

UNIT – 2:

Digital Instruments

Digital Voltmeters – Introduction, DVM's based on V – T, V – F and Successive approximation principles, Resolution and sensitivity, General specifications, Digital Multi-meters, Digital frequency meters, Digital measurement of time.

6 Hrs

UNIT – 3:

Oscilloscopes

Introduction, Basic principles, CRT features, Block diagram and working of each block, Typical CRT connections, Dual beam and dual trace CROs, Electronic switch.

6 Hrs

UNIT – 4:

Special Oscilloscopes

Delayed time-base oscilloscopes, Analog storage, Sampling and Digital storage oscilloscopes.

6 Hrs

UNIT – 5:

Signal Generators

Introduction, Fixed and variable AF oscillator, Standard signal generator, Laboratory type signal generator, AF sine and Square wave generator, Function generator, Square and Pulse generator, Sweep frequency generator, Frequency synthesizer.

6 Hrs

UNIT – 6:

Measurement of resistance, inductance and capacitance

Whetstone's bridge, Kelvin Bridge; AC bridges, Capacitance Comparison Bridge, Maxwell's bridge, Wein's bridge, Wagner's earth connection

5 Hrs

UNIT – 7:

Transducers - I

Introduction, Electrical transducers, Selecting a transducer, Resistive transducer, Resistive position transducer, Strain gauges, Resistance thermometer, Thermistor, Inductive transducer, Differential output transducers and LVDT. **6 Hrs**

UNIT – 8:

Miscellaneous Topics

(a) **Transducers - II** –Piezoelectric transducer, Photoelectric transducer, Photovoltaic transducer, Semiconductor photo devices, Temperature transducers-RTD, Thermocouple .

(b) **Display devices:** Digital display system, classification of display, Display devices, LEDs, LCD displays.

(c) Bolometer and RF power measurement using Bolometer

(d) Introduction to Signal conditioning.

(e) Introduction to LabView. **10 Hrs**

TEXT BOOKS:

1. **“Electronic Instrumentation”**, H. S. Kalsi, TMH, 3rd 2010
2. **“Electronic Instrumentation and Measurements”**, David A Bell, PHI / Pearson Education, 2006.

REFERENCE BOOKS:

1. **“Principles of measurement systems”**, John P. Beatly, 3rd Edition, Pearson Education, 2000
2. **“Modern electronic instrumentation and measuring techniques”**, Cooper D & A D Helfrick, PHI, 1998.
3. **Electronics & electrical measurements**, A K Sawhney, , Dhanpat Rai & sons, 9th edition.

FIELD THEORY
(Common to EC/TC/ML/EE)

Sub Code	:	10ES36	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

UNIT 1:

a. Coulomb’s Law and electric field intensity: Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge. **3 Hrs**

b. Electric flux density, Gauss’ law and divergence: Electric flux density, Gauss’ law, Divergence, Maxwell’s First equation(Electrostatics), vector

operator \square and divergence theorem.

3 Hrs

UNIT 2:

a. Energy and potential : Energy expended in moving a point charge in an electric field, The line integral, Definition of potential difference and Potential, The potential field of a point charge and system of charges, Potential gradient , Energy density in an electrostatic field. **4 Hrs**

b. Conductors, dielectrics and capacitance: Current and current density, Continuity of current, metallic conductors, Conductor properties and boundary conditions, boundary conditions for perfect Dielectrics, capacitance and examples. **4 Hrs**

UNIT 3:

Poisson's and Laplace's equations: Derivations of Poisson's and Laplace's Equations, Uniqueness theorem, Examples of the solutions of Laplace's and Poisson's equations. **6 Hrs**

UNIT 4:

The steady magnetic field: Biot-Savart law, Ampere's circuital law, Curl, Stokes' theorem, magnetic flux and flux density, scalar and Vector magnetic potentials. **6 Hrs**

UNIT 5:

a. Magnetic forces: Force on a moving charge and differential current element, Force between differential current elements, Force and torque on a closed circuit. **4 Hrs**

b. Magnetic materials and inductance: Magnetization and permeability, Magnetic boundary conditions, Magnetic circuit, Potential energy and forces on magnetic materials, Inductance and Mutual Inductance. **4 Hrs**

UNIT 6:

Time varying fields and Maxwell's equations: Faraday's law, displacement current, Maxwell's equation in point and Integral form, retarded potentials. **6 Hrs**

UNIT 7:

Uniform plane wave: Wave propagation in free space and dielectrics, Poynting's theorem and wave power, propagation in good conductors – (skin effect). **6 Hrs**

UNIT 8:

Plane waves at boundaries and in dispersive media: Reflection of uniform plane waves at normal incidence, SWR, Plane wave propagation in general directions. **6 Hrs**

TEXT BOOK:

1. **“Engineering Electromagnetics”**, William H Hayt Jr. and John A Buck, Tata McGraw-Hill, 7th edition, 2006

REFERENCE BOOKS:

1. **“Electromagnetics with Applications”**, John Krauss and Daniel A Fleisch, McGraw-Hill, 5th edition, 1999
2. **“Electromagnetic Waves And Radiating Systems,”** Edward C. Jordan and Keith G Balmain, Prentice – Hall of India / Pearson Education, 2nd edition, 1968.Reprint 2002
3. **“Field and Wave Electromagnetics”**, David K Cheng, Pearson Education Asia, 2nd edition, - 1989, Indian Reprint – 2001.

ANALOG ELECTRONICS LAB
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	10ESL37	IA Marks	:	25
Hrs/ Week	:	03	Exam Hours	:	03
Total Hrs.	:		Exam Marks	:	50

NOTE: Use the Discrete components to test the circuits. LabView can be used for the verification and testing along with the above.

1. Wiring of RC coupled Single stage FET & BJT amplifier and determination of the gain-frequency response, input and output impedances.
2. Wiring of BJT Darlington Emitter follower with and without bootstrapping and determination of the gain, input and output impedances (Single circuit) (One Experiment)
3. Wiring of a two stage BJT Voltage series feed back amplifier and determination of the gain, Frequency response, input and output impedances with and without feedback (One Experiment)
4. Wiring and Testing for the performance of BJT-RC Phase shift Oscillator for $f_0 \leq 10$ KHz
5. Testing for the performance of BJT – Hartley & Colpitts Oscillators for RF range $f_0 \geq 100$ KHz.

6. Testing for the performance of BJT -Crystal Oscillator for $f_0 > 100$ KHz
- 7 Testing of Diode clipping (Single/Double ended) circuits for peak clipping, peak detection
8. Testing of Clamping circuits: positive clamping /negative clamping.
9. Testing of a transformer less Class – B push pull power amplifier and determination of its conversion efficiency.
10. Testing of Half wave, Full wave and Bridge Rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency
11. Verification of Thevinin’s Theorem and Maximum Power Transfer theorem for DC Circuits.
12. Characteristics of Series and Parallel resonant circuits.

LOGIC DESIGN LAB
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	: 10ESL38	IA Marks	: 25
Hrs/ Week	: 03	Exam Hours	: 03
Total Hrs.	:	Exam Marks	: 50

NOTE: Use discrete components to test and verify the logic gates. LabView can be used for designing the gates along with the above.

1. Simplification, realization of Boolean expressions using logic gates/Universal gates.
2. Realization of Half/Full adder and Half/Full Subtractors using logic gates.
3. (i) Realization of parallel adder/Subtractors using 7483 chip
(ii) BCD to Excess-3 code conversion and vice versa.
4. Realization of Binary to Gray code conversion and vice versa
5. MUX/DEMUX – use of 74153, 74139 for arithmetic circuits and code converter.
6. Realization of One/Two bit comparator and study of 7485 magnitude comparator.
7. Use of a) Decoder chip to drive LED display and b) Priority encoder.
8. Truth table verification of Flip-Flops: (i) JK Master slave (ii) T type and (iii) D type.
9. Realization of 3 bit counters as a sequential circuit and MOD – N counter design (7476, 7490, 74192, 74193).

10. Shift left; Shift right, SIPO, SISO, PISO, PIPO operations using 74S95.
11. Wiring and testing Ring counter/Johnson counter.
12. Wiring and testing of Sequence generator.

ENGINEERING MATHEMATICS – IV

Sub Code	:	10MAT41	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

PART-A

UNIT-1

Numerical Methods- 1

Numerical solution of ordinary differential equations of first order and first degree; Picard's method, Taylor's series method, modified Euler's method, Runge-kutta method of fourth-order. Milne's and Adams - Bashforth predictor and corrector methods (No derivations of formulae).

6 Hours

UNIT-2

Numerical Methods – 2

Numerical solution of simultaneous first order ordinary differential equations: Picard's method, Runge-Kutta method of fourth-order.

Numerical solution of second order ordinary differential equations: Picard's method, Runge-Kutta method and Milne's method.

6 Hours

UNIT-3

Complex variables – 1

Function of a complex variable, Analytic functions-Cauchy-Riemann equations in cartesian and polar forms. Properties of analytic functions.

Application to flow problems- complex potential, velocity potential, equipotential lines, stream functions, stream lines.

7 Hours

UNIT-4

Complex variables – 2

Conformal Transformations: Bilinear Transformations. Discussion of

Transformations: $w = z^2$, $w = e^z$, $w = z + (a^2 / z)$. Complex line integrals- Cauchy's theorem and Cauchy's integral formula.

7 Hours

PART-B

UNIT-5

Special Functions

Solution of Laplace equation in cylindrical and spherical systems leading to Bessel's and Legendre's differential equations, Series solution of Bessel's differential equation leading to Bessel function of first kind. Orthogonal property of Bessel functions. Series solution of Legendre's differential equation leading to Legendre polynomials, Rodrigue's formula.

7 Hours

UNIT-6

Probability Theory - 1

Probability of an event, empirical and axiomatic definition, probability associated with set theory, addition law, conditional probability, multiplication law, Baye's theorem.

6 Hours

UNIT-7

Probability Theory- 2

Random variables (discrete and continuous), probability density function, cumulative density function. Probability distributions – Binomial and Poisson distributions; Exponential and normal distributions.

7 Hours

UNIT-

Sampling Theory

Sampling, Sampling distributions, standard error, test of hypothesis for means, confidence limits for means, student's t-distribution. Chi -Square distribution as a test of goodness of fit

6 Hours

Text Books:

1. B.S. Grewal, Higher Engineering Mathematics, Latest edition, Khanna Publishers
2. Erwin Kreyszig, Advanced Engineering Mathematics, Latest edition, Wiley Publications.

Reference Book:

1. B.V. Ramana, Higher Engineering Mathematics, Latest edition, Tata Mc. Graw Hill Publications.
2. Peter V. O'Neil, Engineering Mathematics, CENGAGE Learning India Pvt Ltd.Publishers.

MICROCONTROLLERS
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	10ES42	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

UNIT 1:

Microprocessors and microcontroller. Introduction, Microprocessors and Microcontrollers, RISC & CISC CPU Architectures, Harvard & Von-Neumann CPU architecture, Computer software.

The 8051 Architecture: Introduction, Architecture of 8051, Pin diagram of 8051, Memory organization, External Memory interfacing, Stacks.

6 Hrs

UNIT 2:

Addressing Modes: Introduction, Instruction syntax, Data types, Subroutines, Addressing modes: Immediate addressing , Register addressing, Direct addressing, Indirect addressing, relative addressing, Absolute addressing, Long addressing, Indexed addressing, Bit inherent addressing, bit direct addressing.

Instruction set: Instruction timings, 8051 instructions: Data transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instruction. **6 Hrs**

UNIT 3:

8051 programming: Assembler directives, Assembly language programs and Time delay calculations. **6 Hrs**

UNIT 4:

8051 Interfacing and Applications: Basics of I/O concepts, I/O Port Operation, Interfacing 8051 to LCD, Keyboard, parallel and serial ADC, DAC, Stepper motor interfacing and DC motor interfacing and programming

7 Hrs

UNIT 5:

8051 Interrupts and Timers/counters: Basics of interrupts, 8051 interrupt structure, Timers and Counters, 8051 timers/counters, programming 8051 timers in assembly and C . **6 Hrs**

UNIT 6:

8051 Serial Communication: Data communication, Basics of Serial Data Communication, 8051 Serial Communication, connections to RS-232, Serial communication Programming in assembly and C.

8255A Programmable Peripheral Interface:, Architecture of 8255A, I/O addressing,, I/O devices interfacing with 8051 using 8255A. **6 Hrs**

Course Aim – The MSP430 microcontroller is ideally suited for development of low-power embedded systems that must run on batteries for many years. There are also applications where MSP430 microcontroller must operate on energy harvested from the environment. This is possible due to the ultra-low power operation of MSP430 and the fact that it provides a complete system solution including a RISC CPU, flash memory, on-chip data converters and on-chip peripherals.

UNIT 7:

Motivation for MSP430microcontrollers – Low Power embedded systems, On-chip peripherals (analog and digital), low-power RF capabilities. Target applications (Single-chip, low cost, low power, high performance system design). **2 Hrs**

MSP430 RISC CPU architecture, Compiler-friendly features, Instruction set, Clock system, Memory subsystem. Key differentiating factors between different MSP430 families. **2 Hrs**

Introduction to Code Composer Studio (CCS v4). Understanding how to use CCS for Assembly, C, Assembly+C projects for MSP430 microcontrollers. Interrupt programming. **3 Hrs**

Digital I/O – I/O ports programming using C and assembly, Understanding the muxing scheme of the MSP430 pins. **2 Hrs**

UNIT 8:

On-chip peripherals. Watchdog Timer, Comparator, Op-Amp, Basic Timer, Real Time Clock (RTC), ADC, DAC, SD16, LCD, DMA. **2 Hrs**

Using the Low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and Interrupt. **2 Hrs**

Interfacing LED, LCD, External memory. Seven segment LED modules interfacing. Example – Real-time clock. **2 Hrs**

Case Studies of applications of MSP430 - Data acquisition system, Wired Sensor network, Wireless sensor network with Chipcon RF interfaces. **3 Hrs**

TEXT BOOKS:

1. “**The 8051 Microcontroller and Embedded Systems – using assembly and C**”, Muhammad Ali Mazidi and Janice Gillespie Mazidi and Rollin D. McKinlay; PHI, 2006 / Pearson, 2006
2. “**MSP430 Microcontroller Basics**”, John Davies, Elsevier, 2010
(Indian edition available)

REFERENCE BOOKS:

1. “**The 8051 Microcontroller Architecture, Programming & Applications**”, 2e Kenneth J. Ayala ;, Penram International, 1996 / Thomson Learning 2005.
2. “**The 8051 Microcontroller**”, V.Udayashankar and MalikarjunaSwamy, TMH, 2009
3. **MSP430 Teaching CD-ROM**, Texas Instruments, 2008 (can be requested <http://www.uniti.in>)
4. **Microcontrollers: Architecture, Programming, Interfacing and System Design**”,Raj Kamal, “Pearson Education, 2005

CONTROL SYSTEMS (Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	10ES43	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

UNIT 1:

Modeling of Systems: Introduction to Control Systems, Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems -Mechanical systems, Friction, Translational systems (Mechanical accelerometer, systems excluded), Rotational systems, Gear trains, Electrical systems, Analogous systems. **7 Hrs**

UNIT 2:

Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra, Signal Flow graphs (State variable formulation excluded), **6 Hrs**

UNIT 3:

Time Response of feed back control systems: Standard test signals, Unit step response of First and second order systems, Time response specifications, Time response specifications of second order systems, steady

– state errors and error constants. Introduction to PID Controllers(excluding design) **7 Hrs**

UNIT 4:

Stability analysis: Concepts of stability, Necessary conditions for Stability, Routh- stability criterion, Relative stability analysis; More on the Routh stability criterion. **6 Hrs**

UNIT 5:

Root–Locus Techniques: Introduction, The root locus concepts, Construction of root loci. **6 Hrs**

UNIT 6:

Frequency domain analysis: Correlation between time and frequency response, Bode plots, Experimental determination of transfer functions, Assessment of relative stability using Bode Plots. Introduction to lead, lag and lead-lag compensating networks (excluding design). **7 Hrs**

UNIT 7:

Stability in the frequency domain: Introduction to Polar Plots, (Inverse Polar Plots excluded) Mathematical preliminaries, Nyquist Stability criterion, Assessment of relative stability using Nyquist criterion, (Systems with transportation lag excluded). **7 Hrs**

UNIT 8:

Introduction to State variable analysis: Concepts of state, state variable and state models for electrical systems, Solution of state equations. **6 Hrs**

TEXT BOOK :

1. J. Nagarath and M.Gopal, “Control Systems Engineering”, New Age International (P) Limited, Publishers, Fourth edition – 2005

REFERENCE BOOKS:

1. “**Modern Control Engineering** “, K. Ogata, Pearson Education Asia/ PHI, 4th Edition, 2002.
2. “**Automatic Control Systems**”, Benjamin C. Kuo, John Wiley India Pvt. Ltd., 8th Edition, 2008.
3. “**Feedback and Control System**”, Joseph J Distefano III et al., Schaum’s Outlines, TMH, 2nd Edition 2007.

SIGNALS & SYSTEMS
(Common to EC/TC/IT/BM/ML)

Sub Code	:	10EC44	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

UNIT 1:

Introduction: Definitions of a signal and a system, classification of signals, basic Operations on signals, elementary signals, Systems viewed as Interconnections of operations, properties of systems. **6 Hrs**

UNIT 2:

Time-domain representations for LTI systems – 1: Convolution, impulse response representation, Convolution Sum and Convolution Integral. **6 Hrs**

UNIT 3:

Time-domain representations for LTI systems – 2: Properties of impulse response representation, Differential and difference equation Representations, Block diagram representations. **7 Hrs**

UNIT 4:

Fourier representation for signals – 1: Introduction, Discrete time and continuous time Fourier series (derivation of series excluded) and their properties. **7 Hrs**

UNIT 5:

Fourier representation for signals – 2: Discrete and continuous Fourier transforms(derivations of transforms are excluded) and their properties. **6 Hrs**

UNIT 6:

Applications of Fourier representations: Introduction, Frequency response of LTI systems, Fourier transform representation of periodic signals, Fourier transform representation of discrete time signals. Sampling theorem and Nyquist rate. **7 Hrs**

UNIT 7:

Z-Transforms – 1: Introduction, Z – transform, properties of ROC, properties of Z – transforms, inversion of Z – transforms. **7 Hrs**

UNIT 8:

Z-transforms – 2: Transform analysis of LTI Systems, unilateral Z-

Transform and its application to solve difference equations. **6 Hrs**

TEXT BOOK

1. **Simon Haykin**, “Signals and Systems”, John Wiley India Pvt. Ltd., 2nd Edn, 2008.
2. **Michael Roberts**, “Fundamentals of Signals & Systems”, 2nd ed, Tata McGraw-Hill, 2010

REFERENCE BOOKS:

1. **Alan V Oppenheim, Alan S, Willsky and A Hamid Nawab**, “Signals and Systems” Pearson Education Asia / PHI, 2nd edition, 1997. Indian Reprint 2002
2. **H. P Hsu, R. Ranjan**, “Signals and Systems”, Scham’s outlines, TMH, 2006
3. **B. P. Lathi**, “Linear Systems and Signals”, Oxford University Press, 2005
4. **Ganesh Rao and Satish Tunga**, “Signals and Systems”, Pearson/Sanguine Technical Publishers, 2004

**FUNDAMENTALS OF HDL
(Common to EC/TC/IT/BM/ML)**

Sub Code	:	10EC45	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

UNIT 1:

Introduction: Why HDL? , A Brief History of HDL, Structure of HDL Module, Operators, Data types, Types of Descriptions, simulation and synthesis, Brief comparison of VHDL and Verilog **7 Hrs**

UNIT 2:

Data –Flow Descriptions: Highlights of Data-Flow Descriptions, Structure of Data-Flow Description, Data Type – Vectors. **6 Hrs**

UNIT 3:

Behavioral Descriptions: Behavioral Description highlights, structure of HDL behavioral Description, The VHDL variable –Assignment Statement, sequential statements. **6 Hrs**

UNIT 4:

Structural Descriptions: Highlights of structural Description, Organization of the structural Descriptions, Binding, state Machines, Generate, Generic, and Parameter statements. **7 Hrs**

UNIT 5: Procedures, Tasks, and Functions: Highlights of Procedures, tasks, and Functions, Procedures and tasks, Functions.
Advanced HDL Descriptions: File Processing, Examples of File Processing
7 Hrs

UNIT 6:
Mixed –Type Descriptions: Why Mixed-Type Description? VHDL User-Defined Types, VHDL Packages, Mixed-Type Description examples
6 Hrs

UNIT 7:
Mixed –Language Descriptions: Highlights of Mixed-Language Description, How to invoke One language from the Other, Mixed-language Description Examples, Limitations of Mixed-Language Description. **7 Hrs**

UNIT 8:
Synthesis Basics: Highlights of Synthesis, Synthesis information from Entity and Module, Mapping Process and Always in the Hardware Domain. **6 Hrs**

TEXT BOOKS:

1. **HDL Programming (VHDL and Verilog)-** Nazeih M.Botros- John Wiley India Pvt. Ltd. 2008.

REFERENCE BOOKS:

1. **Fundamentals of HDL** – Cyril P.R. Pearson/Sanguin 2010.
2. **VHDL** –Douglas perry-Tata McGraw-Hill
3. **A Verilog HDL Primer-** J.Bhaskar – BS Publications
4. **Circuit Design with VHDL-**Volnei A.Pedroni-PHI

LINEAR IC's & APPLICATIONS
(Common to EC/TC/IT/BM/ML)

Sub Code	:	10EC46	IA Marks	:	25
Hrs/ Week	:	04	Exam Hours	:	03
Total Hrs.	:	52	Exam Marks	:	100

UNIT 1:

Operational Amplifier Fundamentals: Basic Op-Amp circuit, Op-Amp parameters – Input and output voltage, CMRR and PSRR, offset voltages and currents, Input and output impedances, Slew rate and Frequency limitations; Op-Amps as DC Amplifiers- Biasing Op-Amps, Direct coupled -Voltage Followers, Non-inverting Amplifiers, Inverting amplifiers, Summing amplifiers, Difference amplifier. **7 Hrs**

UNIT 2:

Op-Amps as AC Amplifiers: Capacitor coupled Voltage Follower, High input impedance - Capacitor coupled Voltage Follower, Capacitor coupled Non-inverting Amplifiers, High input impedance - Capacitor coupled Non-inverting Amplifiers, Capacitor coupled Inverting amplifiers, setting the upper cut-off frequency, Capacitor coupled Difference amplifier, Use of a single polarity power supply. **7 Hrs**

UNIT 3:

Op-Amps frequency response and compensation: Circuit stability, Frequency and phase response, Frequency compensating methods, Band width, Slew rate effects, Z_{in} Mod compensation, and circuit stability precautions. **6 Hrs**

UNIT 4:

OP-AMP Applications: Voltage sources, current sources and current sinks, Current amplifiers, instrumentation amplifier, precision rectifiers, Limiting circuits. **6 Hrs**

UNIT 5:

More applications: Clamping circuits, Peak detectors, sample and hold circuits, V to I and I to V converters, Log and antilog amplifiers, Multiplier and divider, Triangular / rectangular wave generators, Wave form generator design, phase shift oscillator, Wein bridge oscillator. **7 Hrs**

UNIT 6:

Non-linear circuit applications: crossing detectors, inverting Schmitt trigger circuits, Monostable & Astable multivibrator, Active Filters –First and second order Low pass & High pass filters. **6 Hrs**

UNIT 7:

Voltage Regulators: Introduction, Series Op-Amp regulator, IC Voltage regulators, 723 general purpose regulator, Switching regulator. **6 Hrs**

UNIT 8:

Other Linear IC applications: 555 timer - Basic timer circuit, 555 timer used as astable and monostable multivibrator, Schmitt trigger; PLL-operating principles, Phase detector / comparator, VCO; D/A and A/ D converters – Basic DAC Techniques, AD converters. **7 Hrs**

TEXT BOOKS:

1. **“Operational Amplifiers and Linear IC’s”**, David A. Bell, 2nd edition, PHI/Pearson, 2004
2. **“Linear Integrated Circuits”**, D. Roy Choudhury and Shail B. Jain, 2nd edition, Reprint 2006, New Age International

REFERENCE BOOKS:

1. **“Opamps- Design, Applications and Trouble Shooting”**, Terrell, Elsevier, 3rd ed. 2006.
2. **“Operational Amplifiers”**, George Clayton and Steve Winder, Elsevier 5th ed., 2008
3. **“Operational Amplifiers and Linear Integrated Circuits”**, Robert. F. Coughlin & Fred.F. Driscoll, PHI/Pearson, 2006
4. **“Design with Operational Amplifiers and Analog Integrated Circuits”**, Sergio Franco, TMH, 3e, 2005

MICROCONTROLLERS LAB
(Common to EC/TC/EE/IT/BM/ML)

Sub Code	:	10ESL47	IA Marks	:	25
Hrs/ Week	:	03	Exam Hours	:	03
Total Hrs.	:	42	Exam Marks	:	50

I. PROGRAMMING

1. Data Transfer - Block move, Exchange, Sorting, Finding largest element in an array.

2. Arithmetic Instructions - Addition/subtraction, multiplication and division, square, Cube – (16 bits Arithmetic operations – bit addressable).
3. Counters.
4. Boolean & Logical Instructions (Bit manipulations).
5. Conditional CALL & RETURN.
6. Code conversion: BCD – ASCII; ASCII – Decimal; Decimal - ASCII; HEX - Decimal and Decimal - HEX .
7. Programs to generate delay, Programs using serial port and on-Chip timer / counter.

Note: Programming exercise is to be done on both 8051 & MSP430.

II. INTERFACING:

Write C programs to interface 8051 chip to Interfacing modules to develop single chip solutions.

8. Simple Calculator using 6 digit seven segment displays and Hex Keyboard interface to 8051.
9. Alphanumeric LCD panel and Hex keypad input interface to 8051.
10. External ADC and Temperature control interface to 8051.
11. Generate different waveforms Sine, Square, Triangular, Ramp etc. using DAC interface to 8051; change the frequency and amplitude.
12. Stepper and DC motor control interface to 8051.
13. Elevator interface to 8051.

HDL LAB (Common to EC/TC/IT/BM/ML)

Sub Code	: 10ECL48	IA Marks	: 25
Hrs/ Week	: 03	Exam Hours	: 03
Total Hrs.	: 42	Exam Marks	: 50

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD boards such as Apex/Acex/Max/Spartan/Sinfi/TK Base or equivalent and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

PROGRAMMING (using VHDL /Verilog)

1. Write HDL code to realize all the logic gates
2. Write a HDL program for the following combinational designs
 - a. 2 to 4 decoder
 - b. 8 to 3 (encoder without priority & with priority)
 - c. 8 to 1 multiplexer
 - d. 4 bit binary to gray converter
 - e. Multiplexer, de-multiplexer, comparator.

3. Write HDL code to accept 8 channel Analog signal, Temperature sensors and display the data on LCD panel or Seven segment display.
 4. Write HDL code to generate different waveforms (Sine, Square, Triangle, Ramp etc.,) using DAC change the frequency and amplitude.
 5. Write HDL code to simulate Elevator operations
 6. Write HDL code to control external lights using relays.
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MANAGEMENT & ENTREPRENEURSHIP

Subject Code	: 10AL51	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

MANAGEMENT

UNIT - 1

MANAGEMENT: Introduction - Meaning - nature and characteristics of Management, Scope and functional areas of Management - Management as a Science, Art or Profession Management & Administration - Roles of Management, Levels of Management, Development of Management Thought-Early Management Approaches-Modern Management Approaches.

7 Hrs

UNIT - 2

PLANNING: Nature, importance and purpose of planning process - Objectives - Types of plans (Meaning only) - Decision making - Importance of planning - steps in planning & planning premises - Hierarchy of plans.

6 Hrs

UNIT - 3

ORGANISING AND STAFFING: Nature and purpose of organization - Principles of organization - Types of organization - Departmentation - Committees – Centralisation Vs Decentralisation of authority and responsibility - Span of control - MBO and MBE (Meaning only) Nature and importance of Staffing - Process of Selection & Recruitment (in brief).

7 Hrs

UNIT - 4

DIRECTING & CONTROLLING: Meaning and nature of directing - Leadership styles, Motivation Theories, Communication - Meaning and importance – Coordination, meaning and importance and Techniques of Co-ordination. Meaning and steps in controlling - Essentials of a sound control system - Methods of establishing control.

6 Hrs

ENTREPRENEURSHIP

UNIT - 5

ENTREPRENEUR: Meaning of Entrepreneur; Evolution of the Concept, Functions of an Entrepreneur, Types of Entrepreneur, Intrapreneur - an emerging Class. Concept of Entrepreneurship - Evolution of

Entrepreneurship, Development of Entrepreneurship; Stages in entrepreneurial process; Role of entrepreneurs in Economic Development; Entrepreneurship in India; Entrepreneurship – its Barriers. **6 Hrs**

UNIT - 6

SMALL SCALE INDUSTRY: Definition; Characteristics; Need and rationale; Objectives; Scope; role of SSI in Economic Development. Advantages of SSI Steps to start an SSI - Government policy towards SSI; Different Policies of S.S.I.; Government Support for S.S.I. during 5 year plans, Impact of Liberalization, Privatization, Globalization on S.S.I., Effect of WTO/GATT Supporting Agencies of Government for S.S.I Meaning; Nature of Support; Objectives; Functions; Types of Help; Ancillary Industry and Tiny Industry (Definition only). **7 Hrs**

UNIT - 7

INSTITUTIONAL SUPPORT: Different Schemes; TECKSOK; KIADB; KSSIDC; KSIMC; DIC Single Window Agency; SISI; NSIC; SIDBI; KSFC. **6 Hrs**

UNIT - 8

PREPARATION OF PROJECT: Meaning of Project; Project Identification; Project Selection; Project Report; Need and Significance of Report; Contents; formulation; Guidelines by Planning Commission for Project report; Network Analysis; Errors of Project Report; Project Appraisal. Identification of Business Opportunities - Market Feasibility Study; Technical Feasibility Study; Financial Feasibility Study & Social Feasibility Study. **7 Hrs**

TEXT BOOKS:

1. **Principles of Management** - P. C. Tripathi, P. N. Reddy; Tata McGraw Hill, 4th Edition, 2010
2. **Dynamics of Entrepreneurial Development & Management** - Vasant Desai Himalaya Publishing House.
3. **Entrepreneurship Development** - Small Business Enterprises - Poornima M Charantimath - Pearson Education – 2006.

REFERENCE BOOKS:

1. **Management Fundamentals** - Concepts, Application, Skill Development Robert Lusier – Thomson.
2. **Entrepreneurship Development** - S S Khanka - S Chand & Co.
3. **Management** - Stephen Robbins - Pearson Education /PHI -17th Edition, 2003.

DIGITAL SIGNAL PROCESSING

Subject Code	: 10EC52	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Discrete Fourier Transforms (DFT): Frequency domain sampling and reconstruction of discrete time signals. DFT as a linear transformation, its relationship with other transforms. **6 Hrs**

UNIT - 2

Properties of DFT, multiplication of two DFTs- the circular convolution, additional DFT properties. **6 Hrs**

UNIT - 3

Use of DFT in linear filtering, overlap-save and overlap-add method. Direct computation of DFT, need for efficient computation of the DFT (FFT algorithms). **7 Hrs**

UNIT - 4

Radix-2 FFT algorithm for the computation of DFT and IDFT—decimation-in-time and decimation-in-frequency algorithms. Goertzel algorithm, and chirp-z transform. **7 Hrs**

UNIT - 5

IIR filter design: Characteristics of commonly used analog filters – Butterworth and Chebyshev filters, analog to analog frequency transformations. **6 Hrs**

UNIT - 6

Implementation of discrete-time systems: Structures for IIR and FIR systems- direct form I and direct form II systems, cascade, lattice and parallel realization. **7 Hrs**

UNIT - 7

FIR filter design: Introduction to FIR filters, design of FIR filters using - Rectangular, Hamming, Bartlett and Kaiser windows, FIR filter design using frequency sampling technique. **6 Hrs**

UNIT - 8

Design of IIR filters from analog filters (Butterworth and Chebyshev) - impulse invariance method. Mapping of transfer functions: Approximation of derivative (backward difference and bilinear transformation) method, Matched z transforms, Verification for stability and linearity during mapping

7 Hrs

TEXT BOOK:

1. **Digital signal processing – Principles Algorithms & Applications**, Proakis & Monalakis, Pearson education, 4th Edition, New Delhi, 2007.

REFERENCE BOOKS:

1. **Discrete Time Signal Processing**, Oppenheim & Schaffer, PHI, 2003.
2. **Digital Signal Processing**, S. K. Mitra, Tata Mc-Graw Hill, 3rd Edition, 2010.
3. **Digital Signal Processing**, Lee Tan: Elsvier publications, 2007

ANALOG COMMUNICATION

Subject Code	: 10EC53	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

RANDOM PROCESS: Random variables: Several random variables. Statistical averages: Function of Random variables, moments, Mean, Correlation and Covariance function: Principles of autocorrelation function, cross – correlation functions. Central limit theorem, Properties of Gaussian process.

7 Hrs

UNIT - 2

AMPLITUDE MODULATION: Introduction, AM: Time-Domain description, Frequency – Domain description. Generation of AM wave: square law modulator, switching modulator. Detection of AM waves: square law detector, envelop detector. Double side band suppressed carrier modulation (DSBSC): Time-Domain description, Frequency-Domain representation, Generation of DSBSC waves: balanced modulator, ring modulator. Coherent detection of DSBSC modulated waves. Costas loop.

7 Hrs

UNIT - 3

SINGLE SIDE-BAND MODULATION (SSB): Quadrature carrier multiplexing, Hilbert transform, properties of Hilbert transform, Pre-envelope, Canonical representation of band pass signals, Single side-band modulation, Frequency-Domain description of SSB wave, Time-Domain description. Phase discrimination method for generating an SSB modulated wave, Time-Domain description. Phase discrimination method for generating an SSB modulated wave. Demodulation of SSB waves. **6 Hrs**

UNIT - 4

VESTIGIAL SIDE-BAND MODULATION (VSB): Frequency – Domain description, Generation of VSB modulated wave, Time - Domain description, Envelop detection of VSB wave plus carrier, Comparison of amplitude modulation techniques, Frequency translation, Frequency division multiplexing, Application: Radio broadcasting, AM radio. **6 Hrs**

UNIT - 5

ANGLE MODULATION (FM)-I: Basic definitions, FM, narrow band FM, wide band FM, transmission bandwidth of FM waves, generation of FM waves: indirect FM and direct FM. **6 Hrs**

UNIT - 6

ANGLE MODULATION (FM)-II: Demodulation of FM waves, FM stereo multiplexing, Phase-locked loop, Nonlinear model of the phase – locked loop, Linear model of the phase – locked loop, Nonlinear effects in FM systems. **7 Hrs**

UNIT - 7

NOISE: Introduction, shot noise, thermal noise, white noise, Noise equivalent bandwidth, Narrow bandwidth, Noise Figure, Equivalent noise temperature, cascade connection of two-port networks. **6 Hrs**

UNIT - 8

NOISE IN CONTINUOUS WAVE MODULATION SYSTEMS: Introduction, Receiver model, Noise in DSB-SC receivers, Noise in SSB receivers, Noise in AM receivers, Threshold effect, Noise in FM receivers, FM threshold effect, Pre-emphasis and De-emphasis in FM,. **7 Hrs**

TEXT BOOKS:

1. **Communication Systems**, Simon Haykins, 5th Edition, John Willey, India Pvt. Ltd, 2009.

2. **An Introduction to Analog and Digital Communication**, Simon Haykins, John Wiley India Pvt. Ltd., 2008

REFERENCE BOOKS:

1. **Modern digital and analog Communication systems** B. P. Lathi, Oxford University Press., 4th ed, 2010,
2. **Communication Systems**, Harold P.E, Stern Samy and A Mahmond, Pearson Edn, 2004.
3. **Communication Systems: Singh and Sapre: Analog and digital** TMH 2nd, Ed 2007.

MICROWAVES AND RADAR

Subject Code	: 10EC54	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

MICROWAVE TRANSMISSION LINES: Introduction, transmission lines equations and solutions, reflection and transmission coefficients, standing waves and SWR, line impedance and line admittance. Smith chart, impedance matching using single stubs, Microwave coaxial connectors.

7 Hrs

UNIT - 2

MICROWAVE WAVEGUIDES AND COMPONENTS: Introduction, rectangular waveguides, circular waveguides, microwave cavities, microwave hybrid circuits, directional couplers, circulators and isolators.

6 Hrs

UNIT - 3

MICROWAVE DIODES,

Transfer electron devices: Introduction, GUNN effect diodes – GaAs diode, RWH theory, Modes of operation, Avalanche transit time devices: READ diode, IMPATT diode, BARITT diode, Parametric amplifiers

Other diodes: PIN diodes, Schottky barrier diodes.

7 Hrs

UNIT - 4

Microwave network theory and passive devices. Symmetrical Z and Y parameters, for reciprocal Networks, S matrix representation of multi port networks.

6 Hrs

UNIT - 5

Microwave passive devices, Coaxial connectors and adapters, Phase shifters, Attenuators, Waveguide Tees, Magic tees. **6 Hrs**

UNIT - 6

STRIP LINES: Introduction, Microstrip lines, Parallel strip lines, Coplanar strip lines, Shielded strip Lines. **6 Hrs**

UNIT - 7

AN INTRODUCTION TO RADAR: Basic Radar, The simple form of the Radar equation, Radar block diagram, Radar frequencies, application of Radar, the origins of Radar. **7 Hrs**

UNIT - 8

MTI AND PULSE DOPPLER RADAR: Introduction to Doppler and MTI Radar, delay line Cancellers, digital MTI processing, Moving target detector, pulse Doppler Radar. **7 Hrs**

TEXT BOOKS:

1. **Microwave Devices and circuits-** Liao / Pearson Education.
2. **Introduction to Radar systems-**Merrill I Skolnik, 3rd Ed, TMH, 2001.
3. **Microwave Engineering** – Annapurna Das, Sisir K Das TMH Publication, 2nd, 2010.

REFERENCE BOOK:

1. **Microwave Engineering** – David M Pozar, John Wiley India Pvt. Ltd., 3rd Edn, 2008.

INFORMATION THEORY AND CODING

Subject Code	: 10EC55	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INFORMATION THEORY: Introduction, Measure of information, Average information content of symbols in long independent sequences, Average information content of symbols in long dependent sequences. Mark-off statistical model for information source, Entropy and information rate of mark-off source. **7 Hrs**

UNIT - 2

SOURCE CODING: Encoding of the source output, Shannon's encoding algorithm. Communication Channels, Discrete communication channels, Continuous channels. **6 Hrs**

UNIT - 3

FUNDAMENTAL LIMITS ON PERFORMANCE: Source coding theorem, Huffman coding, Discrete memory less Channels, Mutual information, Channel Capacity. **7 Hrs**

UNIT - 4

Channel coding theorem, Differential entropy and mutual information for continuous ensembles, Channel capacity Theorem. **6 Hrs**

UNIT - 5

INTRODUCTION TO ERROR CONTROL CODING: Introduction, Types of errors, examples, Types of codes Linear Block Codes: Matrix description, Error detection and correction, Standard arrays and table look up for decoding. **7 Hrs**

UNIT - 6

Binary Cycle Codes, Algebraic structures of cyclic codes, Encoding using an (n-k) bit shift register, Syndrome calculation. BCH codes. **6 Hrs**

UNIT - 7

RS codes, Golay codes, Shortened cyclic codes, Burst error correcting codes. Burst and Random Error correcting codes. **7 Hrs**

UNIT - 8

Convolution Codes, Time domain approach. Transform domain approach. **6 Hrs**

TEXT BOOKS:

1. **Digital and analog communication systems**, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 1996.
2. **Digital communication**, Simon Haykin, John Wiley India Pvt. Ltd, 2008.

REFERENCE BOOKS:

1. **ITC and Cryptography**, Ranjan Bose, TMH, II edition, 2007
2. **Digital Communications** - Glover and Grant; Pearson Ed. 2nd Ed 2008.

FUNDAMENTALS OF CMOS VLSI

Subject Code	: 10EC56	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

BASIC MOS TECHNOLOGY: Integrated circuit's era. Enhancement and depletion mode MOS transistors. nMOS fabrication. CMOS fabrication. Thermal aspects of processing. BiCMOS technology. Production of E-beam masks. **3 Hrs**

MOS TRANSISTOR THEORY: Introduction, MOS Device Design Equations, The Complementary CMOS Inverter – DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate, Tristate Inverter. **4 Hrs**

UNIT - 2

CIRCUIT DESIGN PROCESSES: MOS layers. Stick diagrams. Design rules and layout – lambda-based design and other rules. Examples. Layout diagrams. Symbolic diagrams. Tutorial exercises. **4 Hrs**

Basic Physical Design of Simple logic gates. **3 Hrs**

UNIT - 3

CMOS LOGIC STRUCTURES: CMOS Complementary Logic, Bi CMOS Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic Cascaded Voltage Switch Logic (CVSL). **6 Hrs**

UNIT - 4

BASIC CIRCUIT CONCEPTS: Sheet resistance. Area capacitances. Capacitance calculations. The delay unit. Inverter delays. Driving capacitive loads. Propagation delays. Wiring capacitances. **3 Hrs**

SCALING OF MOS CIRCUITS: Scaling models and factors. Limits on scaling. Limits due to current density and noise. **3 Hrs**

UNIT - 5

CMOS SUBSYSTEM DESIGN: Architectural issues. Switch logic. Gate logic. Design examples – combinational logic. Clocked circuits. Other system considerations. **5 Hrs**

Clocking Strategies **2 Hrs**

UNIT - 6

CMOS SUBSYSTEM DESIGN PROCESSES: General considerations. Process illustration. ALU subsystem. Adders. Multipliers. **6 Hrs**

UNIT - 7

MEMORY, REGISTERS AND CLOCK: Timing considerations. Memory elements. Memory cell arrays. **6 Hrs**

UNIT - 8

TESTABILITY: Performance parameters. Layout issues. I/O pads. Real estate. System delays. Ground rules for design. Test and testability. **7 Hrs**

TEXT BOOKS:

1. **CMOS VLSI Design – A Circuits and Systems Perspective. 3rd Edition.** N.H. Weste and David Harris. Addison-Wesley, 2005. (Refer to <http://www.cmosvlsi.com>)
2. **Principles of CMOS VLSI Design: A Systems Perspective,** Neil H. E. Weste, K. Eshragian, and ??? 3rd edition, Pearson Education (Asia) Pvt. Ltd., 200?. (Shift to the latest edition.)
3. **Basic VLSI Design** - Douglas A. Pucknell & Kamran Eshraghian, PHI 3rd Edition (original Edition – 1994), 2005.

REFERENCE BOOKS:

1. R. Jacob Baker. CMOS Circuit Design, Layout and Simulation. John Wiley India Pvt. Ltd, 2008
2. **Fundamentals of Semiconductor Devices,** M. K. Achuthan and K. N. Bhat, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2007.
3. **CMOS Digital Integrated Circuits: Analysis and Design,** Sung-Mo Kang & Yusuf Leblebici, 3rd Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.
4. **Analysis and Design of Digital Integrated Circuits** - D.A Hodges, H.G Jackson and R.A Saleh. 3rd Edition, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2007.

DIGITAL SIGNAL PROCESSING LABORATORY

Subject Code	: 10ECL57	IA Marks	: 25
No. of Practical Hrs/Week:	03	Exam Hours	: 03
Total no. of Practical Hrs.	: 42	Exam Marks	: 50

A LIST OF EXPERIMENTS USING MATLAB / SCILAB / OCTAVE / WAB

3. Verification of Sampling theorem.
4. Impulse response of a given system
5. Linear convolution of two given sequences.
6. Circular convolution of two given sequences
7. Autocorrelation of a given sequence and verification of its properties.
8. Cross correlation of given sequences and verification of its properties.
9. Solving a given difference equation.
10. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum.
11. Linear convolution of two sequences using DFT and IDFT.
12. Circular convolution of two given sequences using DFT and IDFT
13. Design and implementation of FIR filter to meet given specifications.
14. Design and implementation of IIR filter to meet given specifications.

B. LIST OF EXPERIMENTS USING DSP PROCESSOR

1. Linear convolution of two given sequences.
2. Circular convolution of two given sequences.
3. Computation of N- Point DFT of a given sequence
4. Realization of an FIR filter (any type) to meet given specifications .The input can be a signal from function generator / speech signal.
5. Audio applications such as to plot time and frequency (Spectrum) display of Microphone output plus a cosine using DSP. Read a wav file and match with their respective spectrograms
6. Noise: Add noise above 3kHz and then remove; Interference suppression using 400 Hz tone.
7. Impulse response of first order and second order system

REFERENCE BOOKS:

1. **Digital signal processing using MATLAB** - Sanjeet Mitra, TMH, 2001
2. **Digital signal processing using MATLAB** - J. G. Proakis & Ingale, MGH, 2000
3. **Digital Signal Processors**, B. Venkataramani and Bhaskar, TMH, 2002

ANALOG COMMUNICATION LAB + LIC LAB

Subject Code	: 10ECL58	IA Marks	: 25
No. of Practical Hrs/Week	: 03	Exam Hours	: 03
Total no. of Practical Hrs.	: 42	Exam Marks	: 50

EXPERIMENTS USING DESCERTE COMPONENTS and LABVIEW - 2009 CAN BE USED FOR VERIFICATION AND TESTING.

1. Second order active LPF and HPF
2. Second order active BPF and BE
3. Schmitt Trigger Design and test a Schmitt trigger circuit for the given values of UTP and LTP
4. Frequency synthesis using PLL.
5. Design and test R-2R DAC using op-amp
6. Design and test the following circuits using IC 555
 - a. Astable multivibrator for given frequency and duty cycle
 - b. Monostable multivibrator for given pulse width W
7. IF amplifier design
8. Amplitude modulation using transistor/FET (Generation and detection)
9. Pulse amplitude modulation and detection
10. PWM and PPM
11. Frequency modulation using 8038/2206
12. Precision rectifiers – both Full Wave and Half Wave.

DIGITAL COMMUNICATION

Subject Code	: 10EC61	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Basic signal processing operations in digital communication. Sampling Principles: Sampling Theorem, Quadrature sampling of Band pass signal, Practical aspects of sampling and signal recovery. **7 Hrs**

UNIT - 2

PAM, TDM. Waveform Coding Techniques, PCM, Quantization noise and SNR, robust quantization. **6 Hrs**

UNIT - 3

DPCM, DM, applications. Base-Band Shaping for Data Transmission, Discrete PAM signals, power spectra of discrete PAM signals. **7 Hrs**

UNIT - 4

ISI, Nyquist's criterion for distortion less base-band binary transmission, correlative coding, eye pattern, base-band M-ary PAM systems, adaptive equalization for data transmission. **6 Hrs**

UNIT - 5

DIGITAL MODULATION TECHNIQUES: Digital Modulation formats, Coherent binary modulation techniques, Coherent quadrature modulation techniques. Non-coherent binary modulation techniques. **6 Hrs**

UNIT - 6

Detection and estimation, Model of DCS, Gram-Schmidt Orthogonalization procedure, geometric interpretation of signals, response of bank of correlators to noisy input. **6 Hrs**

UNIT - 7

Detection of known signals in noise, correlation receiver, matched filter receiver, detection of signals with unknown phase in noise. **7 Hrs**

UNIT - 8

Spread Spectrum Modulation: Pseudo noise sequences, notion of spread spectrum, direct sequence spread spectrum, coherent binary PSK, frequency hop spread spectrum, applications. **7 Hrs**

TEXT BOOK:

1. **Digital communications**, Simon Haykin, John Wiley India Pvt. Ltd, 2008.

REFERENCE BOOKS:

1. **Digital and Analog communication systems**, Simon Haykin, John Wiley India Pvt. Ltd, 2008
2. **An introduction to Analog and Digital Communication**, K. Sam Shanmugam, John Wiley India Pvt. Ltd, 2008.
3. **Digital communications** - Bernard Sklar: Pearson education 2007

MICROPROCESSOR

Subject Code	: 10EC62	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

8086 PROCESSORS: Historical background, The microprocessor-based personal computer system, 8086 CPU Architecture, Machine language instructions, Instruction execution timing. **6 Hrs**

UNIT - 2

INSTRUCTION SET OF 8086: Assembler instruction format, data transfer and arithmetic, branch type, loop, NOP & HALT, flag manipulation, logical and shift and rotate instructions. Illustration of these instructions with example programs, Directives and operators. **6 Hrs**

UNIT - 3

BYTE AND STRING MANIPULATION: String instructions, REP Prefix, Table translation, Number format conversions, Procedures, Macros, Programming using keyboard and video display. **7 Hrs**

UNIT - 4

8086 INTERRUPTS: 8086 Interrupts and interrupt responses, Hardware interrupt applications, Software interrupt applications, Interrupt examples. **7 Hrs**

UNIT - 5

8086 INTERFACING: Interfacing microprocessor to keyboard (keyboard types, keyboard circuit connections and interfacing, software keyboard

interfacing, keyboard interfacing with hardware), Interfacing to alphanumeric displays (interfacing LED displays to microcomputer), Interfacing a microcomputer to a stepper motor. **7 Hrs**

UNIT - 6

8086 BASED MULTIPROCESSING SYSTEMS: Coprocessor configurations, The 8087 numeric data processor: data types, processor architecture, instruction set and examples. **6 Hrs**

UNIT - 7

SYSTEM BUS STRUCTURE: Basic 8086 configurations: minimum mode, maximum mode, Bus Interface: peripheral component interconnect (PCI) bus, the parallel printer interface (LPT), the universal serial bus (USB) **6 Hrs**

UNIT - 8

80386, 80486 AND PENTIUM PROCESSORS: Introduction to the 80386 microprocessor, Special 80386 registers, Introduction to the 80486 microprocessor, Introduction to the Pentium microprocessor. **7 Hrs**

TEXT BOOKS:

4. **Microcomputer systems-The 8086 / 8088 Family** – Y.C. Liu and G. A. Gibson, 2E PHI -2003
5. **The Intel Microprocessor, Architecture, Programming and Interfacing**-Barry B. Brey, 6e, Pearson Education / PHI, 2003

REFERENCE BOOKS:

2. **Microprocessor and Interfacing- Programming & Hardware**, Douglas hall, 2nd, TMH, 2006.
3. **Advanced Microprocessors and Peripherals** - A.K. Ray and K.M. Bhurchandi, TMH, 2nd, 2006.
4. **8088 and 8086 Microprocessors - Programming, Interfacing, Software, Hardware & Applications** - Triebel and Avtar Singh, 4e, Pearson Education, 2003

MICROELECTRONICS CIRCUITS

Subject Code : **10EC63**

No. of Lecture Hrs/Week : 04

Total no. of Lecture Hrs. : 52

IA Marks : 25

Exam Hours : 03

Exam Marks : 100

UNIT – 1

MOSFETS: Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, Biasing in MOS amplifier Circuits, Small Signal Operation and Models, MOSFET as an amplifier and as a switch, biasing in MOS amplifier circuits, small signal operation modes, single stage MOS amplifiers. MOSFET internal capacitances and high frequency modes, Frequency response of CS amplifiers, CMOS digital logic inverter, detection type MOSFET. **7 Hrs**

UNIT -2

Single Stage IC Amplifier: IC Design philosophy, Comparison of MOSFET and BJT, Current sources, Current mirrors and Current steering circuits, high frequency response. **6 Hrs**

UNIT – 3

Single Stage IC amplifiers (continued): CS and CF amplifiers with loads, high frequency response of CS and CF amplifiers, CG and CB amplifiers with active loads, high frequency response of CG and CB amplifiers, Cascade amplifiers. CS and CE amplifiers with source (emitter) degeneration source and emitter followers, some useful transfer pairings, current mirrors with improved performance. SPICE examples. **6 Hrs**

UNIT – 4

Differences and Multistage Amplifiers: The MOS differential pair, small signal operation of MOS differential pair, the BJT differences pair, other non-ideal characteristics and differential pair, Differential amplifier with active loads, frequency response and differential amplifiers. Multistage amplifier. SPICE examples. **7 Hrs**

UNIT – 5

Feedback. General Feedback structure. Properties of negative feedback. Four basic feedback topologies. Series-Shunt feedback. Determining the loop gain. Stability problem. Effect of feedback on amplifier poles. Stability study using Bode plots. Frequency compensation. SPICE examples. **7 Hrs**

UNIT - 6

Operational Amplifiers: The two stage CMOS Op-amp, folded cascade CMOS op-amp, 741 op-amp circuit, DC analysis of the 741, small signal analysis of 741, gain, frequency response and slew rate of 741. Data Converters. A-D and D-A converters. **6 Hrs**

UNIT – 7 & 8

Digital CMOS circuits. Overview. Design and performance analysis of CMOS inverter. Logic Gate Circuits. Pass-transistor logic. Dynamic Logic Circuits. SPICE examples. **12 Hrs**

Text Book:

1. “**Microelectronic Circuits**”, Adel Sedra and K.C. Smith, 5th Edition, Oxford University Press, International Version, 2009.

Reference Book:

1. “**Fundamentals of Microelectronics**”, Behzad Razavi, John Wiley India Pvt. Ltd, 2008.
2. “**Microelectronics – Analysis and Design**”, Sundaram Natarajan, Tata McGraw-Hill, 2007

ANTENNAS AND PROPAGATION

Subject Code	: 10EC64	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

ANTENNA BASICS: Introduction, basic Antenna parameters, patterns, beam area, radiation intensity, beam efficiency, diversity and gain, antenna apertures, effective height, bandwidth, radiation, efficiency, antenna temperature and antenna field zones. **7**

Hrs

UNIT - 2

POINT SOURCES AND ARRAYS: Introduction, point sources, power patterns, power theorem, radiation intensity, field patterns, phase patterns. Array of two isotropic point sources. Endfire array and Broadside array. **6**

Hrs

UNIT - 3

ELECTRIC DIPOLES AND THIN LINEAR ANTENNAS: Introduction, short electric dipole, fields of a short dipole (no derivation of field components), radiation resistance of short dipole, radiation resistances of

lambda/2 Antenna, thin linear antenna, micro strip arrays, low side lobe arrays, long wire antenna, folded dipole antennas. **7 Hrs**

UNIT - 4 & 5

LOOP, SLOT, PATCH AND HORN ANTENNA: Introduction, small loop, comparison of far fields of small loop and short dipole, loop antenna general case, far field patterns of circular loop, radiation resistance, directivity, slot antenna, Babinet's principle and complementary antennas, impedance of complementary and slot antennas, patch antennas, horn antennas, rectangular horn antennas. **12 Hrs**

UNIT - 6

ANTENNA TYPES: Helical Antenna, Yagi-Uda array, corner reflectors, parabolic reflectors, log periodic antenna, lens antenna, antenna for special applications – sleeve antenna, turnstile antenna, omni directional antennas, antennas for satellite antennas for ground penetrating radars, embedded antennas, ultra wide band antennas, plasma antenna, high-resolution data, intelligent antennas, antenna for remote sensing. **8 Hrs**

UNIT - 7 & 8

RADIO WAVE PROPAGATION: Introduction, Ground wave propagation, free space propagation, ground reflection, surface wave, diffraction.

TROPOSPHERE WAVE PROPAGATION: Troposcopic scatter, Ionosphere propagation, electrical properties of the ionosphere, effects of earth's magnetic field. **10 Hrs**

TEXT BOOKS:

1. **Antennas and Wave Propagation**, John D. Krauss, 4th Edn, McGraw-Hill International edition, 2010.
2. **Antennas and Wave Propagation** - Harish and Sachidananda: Oxford Press 2007

REFERENCE BOOKS:

1. **Antenna Theory Analysis and Design** - C A Balanis, 3rd Edn, John Wiley India Pvt. Ltd, 2008
2. **Antennas and Propagation for Wireless Communication Systems** - Sineon R Saunders, John Wiley, 2003.
3. **Antennas and wave propagation** - G S N Raju: Pearson Education 2005

OPERATING SYSTEMS

Subject Code	: 10EC65	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION AND OVERVIEW OF OPERATING SYSTEMS:

Operating system, Goals of an O.S, Operation of an O.S, Resource allocation and related functions, User interface related functions, Classes of operating systems, O.S and the computer system, Batch processing system, Multi programming systems, Time sharing systems, Real time operating systems, distributed operating systems.

6 Hrs

UNIT - 2

STRUCTURE OF THE OPERATING SYSTEMS:

Operation of an O.S, Structure of the supervisor, Configuring and installing of the supervisor, Operating system with monolithic structure, layered design, Virtual machine operating systems, Kernel based operating systems, and Microkernel based operating systems.

7 Hrs

UNIT - 3

PROCESS MANAGEMENT: Process concept, Programmer view of processes, OS view of processes, Interacting processes, Threads, Processes in UNIX, Threads in Solaris.

6 Hrs

UNIT - 4

MEMORY MANAGEMENT: Memory allocation to programs, Memory allocation preliminaries, Contiguous and noncontiguous allocation to programs, Memory allocation for program controlled data, kernel memory allocation.

7 Hrs

UNIT - 5

VIRTUAL MEMORY: Virtual memory basics, Virtual memory using paging, Demand paging, Page replacement, Page replacement policies, Memory allocation to programs, Page sharing, UNIX virtual memory.

6 Hrs

UNIT - 6

FILE SYSTEMS: File system and IOCS, Files and directories, Overview of I/O organization, Fundamental file organizations, Interface between file system and IOCS, Allocation of disk space, Implementing file access, UNIX file system.

7 Hrs

UNIT - 7

SCHEDULING: Fundamentals of scheduling, Long-term scheduling, Medium and short term scheduling, Real time scheduling, Process scheduling in UNIX. **6 Hrs**

UNIT - 8

MESSAGE PASSING: Implementing message passing, Mailboxes, Inter process communication in UNIX. **7 Hrs**

TEXT BOOK:

1. **“Operating Systems - A Concept based Approach”**, D. M. Dhamdhare, TMH, 3rd Ed, 2010.

REFERENCE BOOK:

1. **Operating Systems Concepts**, Silberschatz and Galvin, John Wiley India Pvt. Ltd, 5th Edition, 2001.
2. **Operating System – Internals and Design Systems**, Willaim Stalling, Pearson Education, 4th Ed, 2006.
3. **Design of Operating Systems**, Tennambhaum, TMH, 2001.

ADVANCED COMMUNICATION LAB

Subject Code	: 10ECL67	IA Marks	: 25
No. of Practical Hrs/Week:	03	Exam Hours	: 03
Total no. of Practical Hrs.:	42	Exam Marks	: 50

LIST OF EXPERIMENTS USING DESCERTE COMPONENTS and LABVIEW – 2009 can be used for verification and testing.

1. TDM of two band limited signals.
2. ASK and FSK generation and detection
3. PSK generation and detection
4. DPSK generation and detection
5. QPSK generation and detection
6. PCM generation and detection using a CODEC Chip
7. Measurement of losses in a given optical fiber (propagation loss, bending loss) and numerical aperture

8. Analog and Digital (with TDM) communication link using optical fiber.
9. Measurement of frequency, guide wavelength, power, VSWR and attenuation in a microwave test bench
10. Measurement of directivity and gain of antennas: Standard dipole (or printed dipole), microstrip patch antenna and Yagi antenna (printed).
11. Determination of coupling and isolation characteristics of a stripline (or microstrip) directional coupler
12. (a) Measurement of resonance characteristics of a microstrip ring resonator and determination of dielectric constant of the substrate.
(b) Measurement of power division and isolation characteristics of a microstrip 3 dB power divider.

MICROPROCESSOR LAB

Subject Code	: 10ECL68	IA Marks	: 25
No. of Practical Hrs/Week:	03	Exam Hours	: 03
Total no. of Practical Hrs.:	42	Exam Marks	: 50

I) Programs involving

- 1) Data transfer instructions like:
 - i] Byte and word data transfer in different addressing modes.
 - ii] Block move (with and without overlap)
 - iii] Block interchange

- 2) Arithmetic & logical operations like:
 - i] Addition and Subtraction of multi precision nos.
 - ii] Multiplication and Division of signed and unsigned Hexadecimal nos.
 - iii] ASCII adjustment instructions
 - iv] Code conversions
 - v] Arithmetic programs to find square cube, LCM, GCD, factorial

- 3) Bit manipulation instructions like checking:
 - i] Whether given data is positive or negative
 - ii] Whether given data is odd or even
 - iii] Logical 1's and 0's in a given data
 - iv] 2 out 5 code
 - v] Bit wise and nibble wise palindrome

- 4) Branch/Loop instructions like:
 - i] Arrays: addition/subtraction of N nos.
Finding largest and smallest nos.
Ascending and descending order
 - ii] Near and Far Conditional and Unconditional jumps,
Calls and Returns
 - 5) Programs on String manipulation like string transfer, string reversing, searching for a string, etc.
 - 6) Programs involving Software interrupts
Programs to use DOS interrupt INT 21h Function calls for Reading a Character from keyboard, Buffered Keyboard input, Display of character/ String on console
- II) Experiments on interfacing 8086 with the following interfacing modules through DIO (Digital Input/Output-PCI bus compatible) card
- a) Matrix keyboard interfacing
 - b) Seven segment display interface
 - c) Logical controller interface
 - d) Stepper motor interface
- III) Other Interfacing Programs
- a) Interfacing a printer to an X86 microcomputer
 - b) PC to PC Communication

ELECTIVE – GROUP A
ANALOG AND MIXED MODE VLSI DESIGN

Subject Code	: 10EC661	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

(Text Book 1)

UNIT 1

Data converter fundamentals: Analog versus Digital Discrete Time Signals, Converting Analog Signals to Data Signals, Sample and Hold Characteristics, DAC Specifications, ADC Specifications, Mixed-Signal Layout Issues.

7 Hrs

UNIT 2

Data Converters Architectures: DAC Architectures, Digital Input Code, Resistors String, R-2R Ladder Networks, Current Steering, Charge Scaling

DACs, Cyclic DAC, Pipeline DAC, ADC Architectures, Flash, 2-Step Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.

12 Hrs

UNIT 3

Non-Linear Analog Circuits: Basic CMOS Comparator Design (Excluding Characterization), Analog Multipliers, Multiplying Quad (Excluding Stimulation), Level Shifting (Excluding Input Level Shifting For Multiplier).

7 Hrs

(Text Book 2)

UNIT 4:

Data Converter SNR: Improving SNR Using Averaging (Excluding Jitter & Averaging onwards), Decimating Filters for ADCs (Excluding Decimating without Averaging onwards), Interpolating Filters for DAC, Band pass and High pass Sync filters.

8 Hrs

UNIT 5

Su-Microns CMOS circuit design: Process Flow, Capacitors and Resistors, MOSFET Switch (upto Bidirectional Switches), Delay and adder Elements, Analog Circuits MOSFET Biasing (upto MOSFET Transition Frequency).

10 Hrs

UNIT 6

OPAmp Design (Excluding Circuits Noise onwards)

8 Hrs

TEXT BOOK:

1. **Design, Layout, Stimulation** ,R. Jacob Baker, Harry W Li, David E Boyce, CMOS Circuit, PHI Education, 2005
2. **CMOS- Mixed Signal Circuit Design** ,R. Jacob Baker, (Vol II of CMOS: Circuit Design, Layout and Stimulation), John Wiley India Pvt. Ltd, 2008.

REFERENCE BOOKS:

1. **Design of Analog CMOS Integrated Circuits**, B Razavi, First Edition, McGraw Hill,2001.
2. **CMOS Analog Circuit Design**, P e Allen and D R Holberg, 2nd Edition, Oxford University Press,2002.

SATELLITE COMMUNICATION

Subject Code	: 10EC662	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

OVER VIEW OF SATELLITE SYSTEMS: Introduction, frequency allocation, INTEL Sat. **6 Hrs**

UNIT - 2

ORBITS: Introduction, Kepler laws, definitions, orbital element, apogee and perigee heights, orbit perturbations, inclined orbits, calendars, universal time, sidereal time, orbital plane, local mean time and sun synchronous orbits, Geostationary orbit: Introduction, antenna, look angles, polar mix antenna, limits of visibility, earth eclipse of satellite, sun transit outage, leandiaog orbits. **7 Hrs**

UNIT - 3

PROPAGATION IMPAIRMENTS AND SPACE LINK: Introduction, atmospheric loss, ionospheric effects, rain attenuation, other impairments. **SPACE LINK:** Introduction, EIRP, transmission losses, link power budget, system noise, CNR, uplink, down link, effects of rain, combined CNR. **7 Hrs**

UNIT - 4

SPACE SEGMENT: Introduction, power supply units, altitude control, station keeping, thermal control, TT&C, transponders, antenna subsystem. **6 Hrs**

UNIT - 5 & 6

EARTH SEGEMENT: Introduction, receive only home TV system, out door unit, indoor unit, MATV, CATV, Tx – Rx earth station. **5 Hrs**

INTERFERENCE AND SATELLITE ACCESS: Introduction, interference between satellite circuits, satellite access, single access, pre-assigned FDMA, SCPC (spade system), TDMA, pre-assigned TDMA, demand assigned TDMA, down link analysis, comparison of uplink power requirements for TDMA & FDMA, on board signal processing satellite switched TDMA. **9 Hrs**

UNIT - 7 & 8

DBS, SATELLITE MOBILE AND SPECIALIZED SERVICES: Introduction, orbital spacing, power ratio, frequency and polarization,

transponder capacity, bit rates for digital TV, satellite mobile services, USAT, RadarSat, GPS, orb communication and Indian Satellite systems.

12 Hrs

TEXT BOOK:

13. **Satellite Communications**, Dennis Roddy, 4th Edition, McGraw-Hill International edition, 2006.

REFERENCES BOOKS:

3. **Satellite Communications**, Timothy Pratt, Charles Bostian and Jeremy Allnutt, 2nd Edition, John Wiley Pvt. Ltd & Sons, 2008.
4. **Satellite Communication Systems Engineering**, W. L. Pitchand, H. L. Suyderhoud, R. A. Nelson, 2nd Ed., Pearson Education., 2007.

RANDOM PROCESSES

Subject Code	: 10EC663	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION TO PROBABILITY THEORY: Experiments, sample space, Events, Axioms, Assigning probabilities, Joint and conditional probabilities, Baye's Theorem, Independence, Discrete Random Variables, Engg Example.

7 Hrs

UNIT - 2

Random Variables, Distributions, Density Functions: CDF, PDF, Gaussian random variable, Uniform Exponential, Laplace, Gamma, Erlang, Chi-Square, Raleigh, Rician and Cauchy types of random variables.

6 Hrs

UNIT - 3

OPERATIONS ON A SINGLE R V: Expected value, EV of Random variables, EV of functions of Random variables, Central Moments, Conditional expected values.

7 Hrs

UNIT - 4

Characteristic functions, Probability generating functions, Moment generating functions, Engg applications, Scalar quantization, entropy and source coding.

6 Hrs

UNIT - 5

Pairs of Random variables, Joint CDF, joint PDF, Joint probability mass functions, Conditional Distribution, density and mass functions, EV involving pairs of Random variables, Independent Random variables, Complex Random variables, Engg Application. **7 Hrs**

UNIT - 6

MULTIPLE RANDOM VARIABLES: Joint and conditional PMF, CDF, PDF, EV involving multiple Random variables, Gaussian Random variable in multiple dimension, Engg application, linear prediction. **6 Hrs**

UNIT - 7

RANDOM PROCESS: Definition and characterization, Mathematical tools for studying Random Processes, Stationary and Ergodic Random processes, Properties of ACF. **6 Hrs**

UNIT - 8

EXAMPLE PROCESSES: Markov processes, Gaussian Processes, Poisson Processes, Engg application, Computer networks, Telephone networks. **7 Hrs**

TEXT BOOK:

1. **Probability and random processes: application to Signal processing and communication** - S L Miller and D C Childers: Academic Press / Elsevier 2004

REFERENCE BOOKS:

4. **Probability, Random variables and stochastic processes** - A. Papoullis and S U Pillai: McGraw Hill 2002
5. **Probability, Random variables and Random signal principles** - Peyton Z Peebles: TMH 4th Edition 2007
6. **Probability, random processes and applications** - H Stark and Woods: PHI 2001

LOW POWER VLSI DESIGN

Subject Code	: 10EC664	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT – 1

Introduction, Sources of power dissipation, designing for low power. Physics of power dissipation in MOSFET devices – MIS Structure, Long channel and sub-micron MOSFET, Gate induced Drain leakage. **6 Hrs**

UNIT - 2

Power dissipation in CMOS – Short circuit dissipation, dynamic dissipation, Load capacitance. Low power design limits - Principles of low power design, Hierarchy of limits, fundamental limits, Material, device, circuit and system limits.

8 Hrs**UNIT – 3&4**

SYNTHESIS FOR LOW POWER: Behavioral, Logic and Circuit level approaches, Algorithm level transforms, Power-constrained Least squares optimization for adaptive and non-adaptive filters, Circuit activity driven architectural transformations, voltage scaling, operation reduction and substitution, pre- computation, FSM and Combinational logic, Transistor sizing.

12 Hrs**UNIT – 5&6**

DESIGN AND TEST OF LOW-VOLTAGE CMOS CIRCUITS: Introduction, Design style, Leakage current in Deep sub-micron transistors, device design issues, minimizing short channel effect, Low voltage design techniques using reverse V_{gs} , steep sub threshold swing and multiple threshold voltages, Testing with elevated intrinsic leakage, multiple supply voltages.

12 Hrs**UNIT - 7**

LOW ENERGY COMPUTING: Energy dissipation in transistor channel, Energy recovery circuit design, designs with reversible and partially reversible logic, energy recovery in adiabatic logic and SRAM core, Design of peripheral circuits – address decoder, level shifter and I/O Buffer, supply clock generation.

7 Hrs**UNIT - 8**

SOFTWARE DESIGN FOR LOW POWER: Introduction, sources of power dissipation, power estimation and optimization.

7 Hrs**TEXT BOOK:**

1. **Low-Power CMOS VLSI Circuit Design**, Kaushik Roy and Sharat C Prasad, John Wiley Pvt. Ltd, 2008.

DATA STRUCTURE USING C++

Subject Code	: 10EC665	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION: Functions and parameters, Dynamic memory allocation classis, Testing and debugging. Data Representation, Introduction, Linear lists, Formula-based representation linked representation, Indirect addressing simulating pointers. **7 Hrs**

UNIT - 2

ARRAYS AND MATRICES: Arrays, Matrices, Special matrices spare matrices. **6 Hrs**

UNIT - 3

STACKS: The abstract data types, Derived classed and inheritance, Formula-based representation, Linked representation, Applications. **7 Hrs**

UNIT - 4

Queues: The abstract data types, Derived classes and inheritance, Formula-based representation, Linked Linked representation, Applications. **6 Hrs**

UNIT - 5

SKIP LISTS AND HASHING: Dictionaries, Linear representation, Skip list presentation, Hash table representation. **6 Hrs**

UNIT - 6

BINARY AND OTHER TREES: Trees, Binary trees, Properties and representation of binary trees, Common binary tree operations, Binary tree traversal the ADT binary tree, ADT and class extensions. **8 Hrs**

UNIT - 7

PRIRITY QUEUES: Linear lists, Heaps, Leftist trees. **6 Hrs**

UNIT-8

Search Trees: Binary search trees, B-trees, Applications. **6 Hrs**

TEXT BOOK:

1. **Data structures, Algorithms, and applications in C++** - Sartaj Sahni, McGraw Hill.2000.

REFERENCE BOOKS:

1. **Object Oriented Programming in C++** - Balaguruswamy. TMH, 1995.
2. **Programming in C++** - Balaguruswamy. TMH, 4th, 2010 .

DIGITAL SYSTEMS DESIGN USING VERILOG

Subject Code	: 10EC666	IA Marks	: 25
No. of Lecture Hours /week	: 04	Exam Hours	: 03
Total no. of Lecture Hours	: 52	Exam Marks	: 100

UNIT 1

Introduction and Methodology:

Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology. **7 Hrs**

UNIT 2

Combinational Basics:

Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits.

7 Hrs

UNIT 3

Number Basics:

Unsigned and Signed Integers, Fixed and Floating-point Numbers. **6 Hrs**

UNIT 4

Sequential Basics: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology. **6 Hrs**

UNIT 5

Memories: Concepts, Memory Types, Error Detection and Correction.

Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity. **7 Hrs**

UNIT 6

Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory. **6 Hrs**

UNIT 7

I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software. **6 Hrs**

UNIT 8

Accelerators: Concepts, case study, Verification of accelerators.

Design Methodology: Design flow, Design optimization, Design for test,
7 Hrs

Test Book:

1. “**Digital Design: An Embedded Ssystems Approach Using VERILOG**”, Peter J. Ashenden, Elesvier, 2010.

VIRTUAL INSTRUMENTATION

Subject Code	: 10EC668	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT 1

Review of Digital Instrumentation: Representation of analog signals in the digital domain – Review of quantization in amplifier and time areas, sample and hold, sampling theorem, ADC and DAC. **8 Hrs**

UNIT 2 & 3

Fundamentals of Virtual Instrumentation: Concept of Virtual Instrumentation – PC based data acquisition – Typical on board DAQ card – Resolution and sampling frequency – Multiplexing of analog inputs – Single-ended and differential inputs – Different strategies for sampling of multi channel analog inputs. Concept of universal DAQ card – Use of timer-counter and analog outputs on the universal DAQ card. **12 Hrs**

UNIT 4

Cluster of Instruments in System: Interfacing of external instruments to a PC – RS 232C, RS – 422, RS 485 and USB standards – IEEE 488 standard – ISO –OSI model for series bus – introduction to bus protocols of MOD bus and CAN bus. **8 Hrs**

UNIT 5 & 6

Graphical Programming Environment in VI: Concepts of graphical programming – Lab-view software – Concept of VIs and sub VIs – Display types – Digital – Analog – Chart – Oscilloscope types – Loops – Case and sequence structures – Types of data – Arrays – Formulate nodes – Local and Global variables – String and file I/O. **12 Hrs**

UNIT 7 & 8

Analysis Tools and Simple Application in VI: Fourier transform – Power spectrum – Correlation – Windowing and filtering tools – Simple temperature indicator – ON/OFF controller – PID controller – CRO emulation – Simulation of a simple second order system – Generation of HTML page. **12 Hrs**

Text Books:

1. Sanjay Gupta, “**Virtual Instrumentation, LABVIEW**”, TMH, New Delhi, 2003
2. S. Gupta and J P Gupta, “**PC Interfacing for Data Acquisition and Process Control**”, Instrument Society of America, 1994

Reference Books:

3. Peter W Gofton , “**Understanding Serial Communication**”, Sybes International, 2000
4. Robert H. Bishop, “**Learning with Lab-View**” Prentice Hall, 2009
5. Ernest O. Doebelin and Dhanesh N Manik, “ **Measurement Systems – Application and Design**”, 5th Edn, TMH, 2007.

**VII SEMESTER
COMPUTER COMMUNICATION NETWORKS**

Subject Code	: 10EC71	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Layered tasks, OSI Model, Layers in OSI model, TCP/IP Suite, Addressing, Telephone and cable networks for data transmission, Telephone networks, Dial up modem, DSL, Cable TV for data transmission. **7 Hrs**

UNIT - 2

DATA LINK CONTROL: Framing, Flow and error control, Protocols, Noiseless channels and noisy channels, HDLC. **6 Hrs**

UNIT - 3

MULTIPLE ACCESSES: Random access, Controlled access, Channelisation. **6 Hrs**

UNIT - 4

Wired LAN, Ethernet, IEEE standards, Standard Ethernet. Changes in the standards, Fast Ethernet, Gigabit Ethernet, Wireless LAN IEEE 802.11 **7 Hrs**

UNIT - 5

Connecting LANs, Backbone and Virtual LANs, Connecting devices, Backbone Networks, Virtual LANs **7 Hrs**

UNIT - 6

Network Layer, Logical addressing, Ipv4 addresses, Ipv6 addresses, Ipv4 and Ipv6 Transition from Ipv4 to Ipv6. **6 Hrs**

UNIT - 7

Delivery, Forwarding, Unicast Routing Protocols, Multicast Routing protocols. **6 Hrs**

UNIT - 8

Transport layer Process to process Delivery, UDP, TCP, Domain name system, Resolution. **7 Hrs**

TEXT BOOK:

1. **Data Communication and Networking**, B Forouzan, 4th Ed, TMH 2006

REFERENCE BOOKS:

4. **Computer Networks**, James F. Kurose, Keith W. Ross: Pearson education, 2nd Edition, 2003
5. **Introduction to Data communication and Networking**, Wayne Tomasi: Pearson education 2007

OPTICAL FIBER COMMUNICATION

Subject Code	: 10EC72	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

OVERVIEW OF OPTICAL FIBER COMMUNICATION: Introduction, Historical development, general system, advantages, disadvantages, and applications of optical fiber communication, optical fiber waveguides, Ray theory, cylindrical fiber (no derivations in article 2.4.4), single mode fiber, cutoff wave length, mode field diameter. Optical Fibers: fiber materials, photonic crystal, fiber optic cables specialty fibers. **7 Hrs**

UNIT - 2

TRANSMISSION CHARACTERISTICS OF OPTICAL FIBERS: Introduction, Attenuation, absorption, scattering losses, bending loss, dispersion, Intra model dispersion, Inter model dispersion. **6 Hrs**

UNIT - 3

OPTICAL SOURCES AND DETECTORS: Introduction, LED's, LASER diodes, Photo detectors, Photo detector noise, Response time, double hetero junction structure, Photo diodes, comparison of photo detectors. **6 Hrs**

UNIT - 4

FIBER COUPLERS AND CONNECTORS: Introduction, fiber alignment and joint loss, single mode fiber joints, fiber splices, fiber connectors and fiber couplers. **6 Hrs**

UNIT - 5

OPTICAL RECEIVER: Introduction, Optical Receiver Operation, receiver sensitivity, quantum limit, eye diagrams, coherent detection, burst mode receiver, operation, Analog receivers. **6 Hrs**

UNIT - 6

ANALOG AND DIGITAL LINKS: Analog links – Introduction, overview of analog links, CNR, multichannel transmission techniques, RF over fiber, key link parameters, Radio over fiber links, microwave photonics. Digital links – Introduction, point-to-point links, System considerations, link power budget, resistive budget, short wave length band, transmission distance for single mode fibers, Power penalties, nodal noise and chirping. **8 Hrs**

UNIT - 7

WDM CONCEPTS AND COMPONENTS: WDM concepts, overview of WDM operation principles, WDM standards, Mach-Zehender interferometer, multiplexer, Isolators and circulators, direct thin film filters, active optical components, MEMS technology, variable optical attenuators, tunable optical fibers, dynamic gain equalizers, optical drop multiplexers, polarization controllers, chromatic dispersion compensators, tunable light sources. **7 Hrs**

UNIT - 8

Optical Amplifiers and Networks – optical amplifiers, basic applications and types, semiconductor optical amplifiers, EDFA.
OPTICAL NETWORKS: Introduction, SONET / SDH, Optical Interfaces, SONET/SDH rings, High – speed light – waveguides. **6 Hrs**

TEXT BOOKS:

1. "**Optical Fiber Communication**", Gerd Keiser, 4th Ed., MGH, 2008.
2. "**Optical Fiber Communications**", John M. Senior, Pearson Education. 3rd Impression, 2007.

REFERENCE BOOK:

1. **Fiber Optic Communication** - Joseph C Palais: 4th Edition, Pearson Education.

POWER ELECTRONICS

Subject Code	: 10EC73	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Introduction, Applications of power electronics, Power semiconductor devices, Control characteristics, Types of power electronics circuits, Peripheral effects.

6 Hrs**UNIT - 2**

POWER TRANSISTOR: Power BJT's, Switching characteristics, Switching limits, Base drive control, Power MOSFET's, Switching characteristics, Gate drive, IGBT's, Isolation of gate and base drives.

6 Hrs**UNIT - 3**

INTRODUCTION TO THYRISTORS: Principle of operation states anode-cathode characteristics, Two transistor model. Turn-on Methods, Dynamic Turn-on and turn-off characteristics, Gate characteristics, Gate trigger circuits, di/dt and dv/dt protection, Thyristor firing circuits.

7 Hrs**UNIT - 4**

CONTROLLED RECTIFIERS: Introduction, Principles of phase controlled converter operation, 1ϕ fully controlled converters, Dual converters, 1ϕ semi converters (all converters with R & RL load).

7 Hrs**UNIT - 5**

Thyristor turn off methods, natural and forced commutation, self commutation, class A and class B types, Complementary commutation, auxiliary commutation, external pulse commutation, AC line commutation, numerical problems.

7 Hrs

UNIT - 6

AC VOLTAGE CONTROLLERS: Introduction, Principles of on and off control, Principles of phase control, Single phase controllers with resistive loads and Inductive loads, numerical problems. **6 Hrs**

UNIT - 7

DC CHOPPERS: Introduction, Principles of step down and step up choppers, Step down chopper with RL loads, Chopper classification, Switch mode regulators – buck, boost and buck – boost regulators. **6 Hrs**

UNIT - 8

INVERTORS: Introduction, Principles of operation, Performance parameters, 1ϕ bridge inverter, voltage control of 1ϕ invertors, current source invertors, Variable DC link inverter.

7 Hrs

TEXT BOOKS:

4. **“Power Electronics”** - M. H. Rashid 3rd edition, PHI / Pearson publisher 2004.
5. **“Power Electronics”** - M. D. Singh and Kanchandani K.B. TMH publisher, 2nd Ed. 2007.

REFERENCE BOOKS:

6. **“Power Electronics, Essentials and Applications”, L Umanand,** John Wiley India Pvt. Ltd, 2009.
7. **“Power Electronics”**, Daniel W. Hart, McGraw Hill, 2010.
8. **“Power Electronics”, V Nattarasu and R.S. Anandamurthy,** Pearson/Sanguine Pub. 2006.

EMBEDED SYSTEM DESIGN

Subject Code	: 10EC74	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT 1:

Introduction to Embedded System: Introducing Embedded Systems, Philosophy, Embedded Systems, Embedded Design and Development Process. **5 Hrs**

UNIT 2:

The Hardware Side: An Introduction, The Core Level, Representing Information, Understanding Numbers, Addresses, Instructions, Registers-A First Look, Embedded Systems-An Instruction Set View, Embedded Systems-A Register View, Register View of a Microprocessor
The Hardware Side: Storage Elements and Finite-State Machines (2 hour)
The concepts of State and Time, The State Diagram, Finite State Machines-A Theoretical Model. **8 Hrs**

UNIT 3:

Memories and the Memory Subsystem: Classifying Memory, A General Memory Interface, ROM Overview, Static RAM Overview, Dynamic RAM Overview, Chip Organization, Terminology, A Memory Interface in Detail, SRAM Design, DRAM Design, DRAM Memory Interface, The Memory Map, Memory Subsystem Architecture, Basic Concepts of Caching, Designing a Cache System, Dynamic Memory Allocation. **7 Hrs**

UNIT 4:

Embedded Systems Design and Development : System Design and Development, Life-cycle Models, Problem Solving-Five Steps to Design, The Design Process, Identifying the Requirements, Formulating the Requirements Specification, The System Design Specification, System Specifications versus System Requirements, Partitioning and Decomposing a System, Functional Design, Architectural Design, Functional Model versus Architectural Model, Prototyping, Other Considerations, Archiving the Project. **6 Hrs**

UNIT 5 & 6:

Real-Time Kernels and Operating Systems: Tasks and Things, Programs and Processes, The CPU is a resource, Threads – Lightweight and heavyweight, Sharing Resources, Foreground/Background Systems, The operating System, The real time operating system (RTOS), OS architecture, Tasks and Task control blocks, memory management revisited. **12 Hrs**

UNIT 7 & 8:

Performance Analysis and Optimization: Performance or Efficiency Measures, Complexity Analysis, The methodology, Analyzing code, Instructions in Detail, Time, etc. – A more detailed look, Response Time, Time Loading, Memory Loading, Evaluating Performance, Thoughts on Performance Optimization, Performance Optimization, Tricks of the Trade, Hardware Accelerators, Caches and Performance. **12 Hrs**

Text Book:

1. **Embedded Systems – A contemporary Design**

Tool, James K. Peckol, John Wiley India Pvt. Ltd, 2008

Reference Books:

1. **Embedded Systems: Architecture and Programming**, Raj Kamal, TMH, 2008
2. **Embedded Systems Architecture – A Comprehensive Guide for Engineers and Programmers**, Tammy Noergaard, Elsevier Publication, 2005
3. **Programming for Embedded Systems**, Dreamtech Software Team, John Wiley India Pvt. Ltd, 2008

VLSI LAB

Subject Code	: 10ECL77	IA Marks	: 25
No. of Practical Hrs/Week	: 03	Exam Hours	: 03
Total no. of Practical Hrs.	: 42	Exam Marks	: 50

(Wherever necessary Cadence/Synopsis/Menta Graphics tools must be used)

PART - A

DIGITAL DESIGN

ASIC-DIGITAL DESIGN FLOW

1. Write Verilog Code for the following circuits and their Test Bench for **verification**, observe the waveform and **synthesize** the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.

1. An inverter
2. A Buffer
3. Transmission Gate
4. Basic/universal gates
5. Flip flop -RS, D, JK, MS, T
6. Serial & Parallel adder
7. 4-bit counter [Synchronous and Asynchronous counter]
8. Successive approximation register [SAR]

** An appropriate constraint should be given*

PART - B
ANALOG DESIGN

Analog Design Flow

1. Design an **Inverter** with given specifications*, completing the design flow mentioned below:
 - a. **Draw the schematic** and verify the following
 - i) DC Analysis
 - ii) Transient Analysis
 - b. **Draw the Layout** and verify the DRC, ERC
 - c. Check for LVS
 - d. Extract RC and back annotate the same and verify the Design
 - e. Verify & Optimize for Time, Power and Area to the given constraint***

2. Design the following circuits with given specifications*, completing the design flow mentioned below:
 - a. Draw the schematic and verify the following
 - i) DC Analysis
 - ii) AC Analysis
 - iii) Transient Analysis
 - b. Draw the Layout and verify the DRC, ERC
 - c. Check for LVS
 - d. Extract RC and back annotate the same and verify the Design.
 - i) A Single Stage differential amplifier
 - ii) Common source and Common Drain amplifier

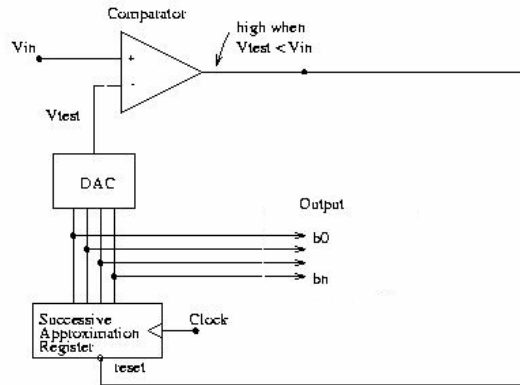
3. Design an **op-amp** with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:
 - a. Draw the schematic and verify the following
 - i) DC Analysis
 - ii). AC Analysis
 - iii) Transient Analysis
 - b. Draw the Layout and verify the DRC, ERC
 - c. Check for LVS
 - d. Extract RC and back annotate the same and verify the Design.

4. Design a **4 bit R-2R based DAC** for the given specification and completing the design flow mentioned using given op-amp in the library**.
 - a. Draw the schematic and verify the following

- i) DC Analysis
- ii) AC Analysis
- iii) Transient Analysis
- b. Draw the Layout and verify the DRC, ERC
- c. Check for LVS
- d. Extract RC and back annotate the same and verify the Design.

5. For the **SAR based ADC** mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW.

[Specifications to GDS-II]



- * Appropriate specification should be given.
- ** Applicable Library should be added & information should be given to the Designer.
- *** An appropriate constraint should be given

POWER ELECTRONICS LAB

Subject Code	: 10ECL78	IA Marks	: 25
No. of Practical Hrs/Week:	03	Exam Hours	: 03
Total no. of Practical Hrs. :	42	Exam Marks	: 50

Any five converter circuits experiment from the below list **must be** simulated using the **spice-simulator**.

- Static characteristics of SCR and DIAC.
- Static characteristics of MOSFET and IGBT.
- Controlled HWR and FWR using RC triggering circuit
- SCR turn off using i) LC circuit ii) Auxiliary Commutation
- UJT firing circuit for HWR and FWR circuits.
- Generation of firing signals for thyristors/ triacs using digital circuits / microprocessor.
- AC voltage controller using triac – diac combination.
- Single phase Fully Controlled Bridge Converter with R and R-L loads.
- Voltage (Impulse) commutated chopper both constant frequency and variable frequency operations.
- Speed control of a separately excited DC motor.
- Speed control of universal motor.
- Speed control of stepper motor.
- Parallel / series inverter.

Note: Experiments to be conducted with isolation transformer and low voltage.

DSP ALGORITHMS AND ARCHITECTURE

Subject Code	: 10EC751	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION TO DIGITAL SIGNAL PROCESSING: Introduction, A Digital Signal-Processing System, The Sampling Process, Discrete Time Sequences, Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear Time-Invariant Systems, Digital Filters, Decimation and Interpolation. **6 Hrs**

UNIT - 2

ARCHITECTURES FOR PROGRAMMABLE DIGITAL SIGNAL-PROCESSORS: Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing. **7 Hrs**

UNIT - 3

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Introduction,

Commercial Digital Signal-processing Devices, Data Addressing Modes of TMS320C54xx., Memory Space of TMS320C54xx Processors, Program Control. **6 Hrs**

UNIT - 4

Detail Study of TMS320C54X & 54xx Instructions and Programming, On-Chip peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54xx Processor. **7 Hrs**

UNIT - 5

IMPLEMENTATION OF BASIC DSP ALGORITHMS: Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). **7 Hrs**

UNIT - 6

IMPLEMENTATION OF FFT ALGORITHMS: Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit-Reversed Index Generation & Implementation on the TMS320C54xx. **6 Hrs**

UNIT - 7

INTERFACING MEMORY AND PARALLEL I/O PERIPHERALS TO DSP DEVICES: Introduction, Memory Space Organization, External Bus Interfacing Signals. Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I / O Direct Memory Access (DMA). **6 Hrs**

UNIT - 8

INTERFACING AND APPLICATIONS OF DSP PROCESSOR: Introduction, Synchronous Serial Interface, A CODEC Interface Circuit. DSP Based Bio-telemetry Receiver, A Speech Processing System, An Image Processing System. **7 Hrs**

TEXT BOOK:

4. **“Digital Signal Processing”**, Avatar Singh and S. Srinivasan, Thomson Learning, 2004.

REFERENCE BOOKS:

1. **Digital Signal Processing: A practical approach**, Iffachor E. C., Jervis B. W Pearson-Education, PHI/ 2002
2. **“Digital Signal Processors”**, B Venkataramani and M Bhaskar TMH, 2nd, 2010
3. **“Architectures for Digital Signal Processing”**, Peter Pirsch John Wiley, 2008

MICRO AND SMART SYSTEMS TECHNOLOGY

Subject Code	: 10MS752	IA Marks	: 25
No. of Lecture Hrs./ Week	: 04	Exam Hours	: 03
Total No. of Lecture Hrs.	: 52	Exam Marks	: 10
			0

UNIT - 1

INTRODUCTION TO MICRO AND SMART SYSTEMS:

- What are smart-material systems? Evolution of smart materials, structures and systems. Components of a smart system. Application areas. Commercial products.
- What are microsystems? Feynman's vision. Micromachined transducers. Evolution of micro-manufacturing. Multi-disciplinary aspects. Applications areas. Commercial products.

6 Hrs

UNIT - 2

MICRO AND SMART DEVICES AND SYSTEMS: PRINCIPLES AND MATERIALS:

- Definitions and salient features of sensors, actuators, and systems.
- Sensors: silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conductometric gas sensor, fiber-optic gyroscope and surface-acoustic-wave based wireless strain sensor.
- Actuators: silicon micro-mirror arrays, piezo-electric based inkjet print-head, electrostatic comb-drive and micromotor, magnetic micro relay, shape-memory-alloy based actuator, electro-thermal actuator.
- Systems: micro gas turbine, portable clinical analyzer, active noise control in a helicopter cabin.

7 Hrs

UNIT - 3

MICROMANUFACTURING AND MATERIAL PROCESSING:

- Silicon wafer processing, lithography, thin-film deposition, etching (wet and dry), wafer-bonding, and metallization.
- Silicon micromachining: surface, bulk, moulding, bonding based process flows.
- Thick-film processing:
- Smart material processing:
- Processing of other materials: ceramics, polymers and metals
- Emerging trends.

7 Hrs

UNIT - 4

MODELING:

- a. Scaling issues.
- b. Elastic deformation and stress analysis of beams and plates. Residual stresses and stress gradients. Thermal loading. Heat transfer issues. Basic fluids issues.
- c. Electrostatics. Coupled electromechanics. Electromagnetic actuation. Capillary electro-phoresis. Piezoresistive modeling. Piezoelectric modeling. Magnetostrictive actuators.

6 Hrs

UNIT - 5

COMPUTER-AIDED SIMULATION AND DESIGN:

Background to the finite element method. Coupled-domain simulations using Matlab. Commercial software.

6 Hrs

UNIT - 6

ELECTRONICS, CIRCUITS AND CONTROL:

Carrier concentrations, semiconductor diodes, transistors, MOSFET amplifiers, operational amplifiers. Basic Op-Amp circuits. Charge-measuring circuits. Examples from microsystems. Transfer function, state-space modeling, stability, PID controllers, and model order reduction. Examples from smart systems and micromachined accelerometer or a thermal cyler.

7 Hrs

UNIT - 7

INTEGRATION AND PACKAGING OF MICROELECTRO MECHANICAL SYSTEMS:

Integration of microelectronics and micro devices at wafer and chip levels. Microelectronic packaging: wire and ball bonding, flip-chip. Low-temperature-cofired-ceramic (LTCC) multi-chip-module technology. Microsystem packaging examples.

7 Hrs

UNIT - 8

CASE STUDIES:

BEL pressure sensor, thermal cyler for DNA amplification, and active vibration control of a beam.

6 Hrs

UNIT - 9

Mini-projects and class-demonstrations (not for Examination)

- a) CAD lab (coupled field simulation of electrostatic-elastic actuation with fluid effect)

- b) BEL pressure sensor
- c) Thermal-cycler for PCR
- d) Active control of a cantilever beam

TEXT BOOKS AND A CD-SUPPLEMENT:

- 1. **MEMS & Microsystems: Design and Manufacture**, Tai-Ran Tsu, Tata Mc-Graw-Hill.
- 2. **“Micro and Smart Systems”** by Dr. A.K.Aatre, Prof. Ananth Suresh, Prof.K.J.Vinoy, Prof. S. Gopalakrishna,, Prof. K.N.Bhat.,John Wiley Publications.

REFERENCE BOOKS:

- 2. Animations of working principles, process flows and processing techniques, A CD-supplement with Matlab codes, photographs and movie clips of processing machinery and working devices.
- 3. **Laboratory hardware kits for** (i) BEL pressure sensor, (ii) thermal-cycler and (iii) active control of a cantilever beam.
- 1. **Microsystems Design**, S. D. Senturia, 2001, Kluwer Academic Publishers, Boston, USA. ISBN 0-7923-7246-8.
- 2. **Analysis and Design Principles of MEMS Devices**, Minhang Bao, Elsevier, Amsterdam, The Netherlands, ISBN 0-444-51616-6.
- 3. **Design and Development Methodologies**, Smart Material Systems and MEMS: V. Varadan, K. J. Vinoy, S. Gopalakrishnan, Wiley.
- 4. **MEMS-** Nitaigour Premchand Mahalik, TMH 2007

ARTIFICIAL NEURAL NETWORKS

Subject Code	: 10EC753	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Introduction, history, structure and function of single neuron, neural net architectures, neural learning, use of neural networks. **6 Hrs**

UNIT - 2

Supervised learning, single layer networks, perceptions, linear separability, perceptions training algorithm, guarantees of success, modifications. **7 Hrs**

UNIT - 3

Multiclass networks-I, multilevel discrimination, preliminaries, back propagation, setting parameter values, theoretical results. **7 Hrs**

UNIT - 4

Accelerating learning process, application, mandaline, adaptive multilayer networks. **6 Hrs**

UNIT - 5

Prediction networks, radial basis functions, polynomial networks, regularization, unsupervised learning, winner take all networks. **6 Hrs**

UNIT - 6

Learning vector quantizing, counter propagation networks, adaptive resonance theorem, topologically organized networks, distance based learning, neo-cognition. **7 Hrs**

UNIT - 7

Associative models, hop field networks, brain state networks, Boltzmann machines, hetero associations. **6 Hrs**

UNIT - 8

Optimization using hop filed networks, simulated annealing, random search, evolutionary computation. **7 Hrs**

TEXT BOOK:

1. **Elements of Artificial Neural Networks**, Kishan Mehrotra, C. K. Mohan, Sanjay Ranka, Penram, 1997.

REFERENCE BOOKS:

1. **Artificial Neural Networks**, R. Schalkoff, MGH, 1997.
2. **Introduction to Artificial Neural Systems**, J. Zurada, Jaico, 2003.
3. **Neural Networks**, Haykins, Pearson Edu., 1999.

CAD FOR VLSI

Subject Code	: 10EC754	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT – 1&2

INTRODUCTION TO VLSI METHODOLOGIES: VLSI Physical Design Automation - Design and Fabrication of VLSI Devices - Fabrication process and its impact on Physical Design. **12 Hrs**

UNIT – 3&4

A QUICK TOUR OF VLSI DESIGN AUTOMATION TOOLS: Data structures and Basic Algorithms, Algorithmic Graph theory and computational complexity, Tractable and Intractable problems. **14 Hrs**

UNIT – 5&6

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: partitioning, floor planning and pin assignment, placement, routing. **14 Hrs**

UNIT – 7&8

SIMULATION-LOGIC SYNTHESIS: Verification-High level synthesis - Compaction. Physical Design Automation of FPGAs, MCMS-VHDL-Verilog-Implementation of Simple circuits using VHDL and Verilog. **12 Hrs**

REFERENCE BOOKS:

1. **“Algorithms for VLSI Physical Design Automation”**, N. A. Shervani, 1999.
2. **“Algorithms for VLSI Design Automation”**, S. H. Gerez, 1998.

APPLIED EMBEDDED SYSTEM DESIGN

Subject Code	: 10EC755	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

PART-A

Unit 1. Introduction to the Embedded Systems:

An embedded System, Processor embedded into a system (A). Embedded Hardware Units and devices in a system, Embedded software in a system, Examples of embedded systems, Embedded system-on-chip (SoC) and use of VLSI circuits design technology (A), Complex systems design and processors, Design process in embedded system, Formalism of system design, Design process and design examples, Classification of embedded systems. Skills required for an embedded system designer. **5**

Hours

Unit 2. 8051 and Advanced Processor Architecture:

8051 Architecture, Real world interfacing, Introduction to advanced architecture
Processor and memory architecture, Instruction level parallelism, Performance metrics
Memory types and addresses, Processor selection, Memory selection
5 Hours

Unit 3. Devices and Communication Buses for Devices Network:

Devices and Communication buses for Networks, Serial communication devices
Parallel port devices, Sophisticated interfacing features in device ports, Wireless communication devices, Timer and counting devices, Watchdog timers, Real time clocks
Parallel bus device protocols – parallel communication network using the ISA, PCI, PCI-X and advanced buses, Wireless and mobile system protocols.
6 Hours

Unit 4. Device drivers and interrupts servicing mechanism:

Port or device access without interrupt servicing mechanism, Interrupt service routine, thread and device driver concept, Interrupt sources, Interrupt servicing (handling) mechanism

Multiple interrupts, Context and the periods for context-switching, interrupt latency and
Deadline Classification of processors interrupt service mechanism from context saving angle
Direct memory access, Device driver programming, Parallel port device drivers in a system
Serial port device drivers in a system, Timer devices and devices interrupts
8 Hours

PART-B

Unit 5. Programming concepts and embedded programming in C, C++ and Java:

Software programming in assembly language (ALP) and in high level language 'C'

'C' programming elements: header and source files and preprocessor directives

Program elements : macros and functions, Program elements: data types, data structures,

modifiers, statements, loops and pointers, Objected oriented programming

Embedded programming in Java, Optimisation of Memory needs.

5 Hours

Unit 6. Program modeling concepts in single and multiprocessor systems software – development process:

Program models, Data flow graph models, State machine programming models for event

controlled programs, Modeling of multiprocessor systems, UML modeling
5 Hours

Unit 7. Real time operating systems – I: Inter process communication and synchronization of processes, Task and Threads):

Multiple processes in an application, Multiple threads in an applications, Task

Tasks and states, Tasks and data, Clear cut distinction between Functions, ISRs and Tasks by

their Characteristics, Concept of semaphores, Shared data, Inter process communications

Signals, Semaphores, Message queues, Mailboxes, Pipes, Sockets,
Remote procedure calls
(RPCs).

8 Hours

Unit 8. Real time operating systems:

Operating system service, Process management, Timer
functions, Event functions,
Memory management, Device, file and IO subsystems management
Interrupt routines in RTOS environment and handling of interrupt
source calls by RTOS
Introduction to Real Time Operating System, Basic design using a
Real Time Operating
System, RTOS Task Scheduling Models, Latency, Response Times,
Deadline as Performance
Metric, OS security issues, IEEE Standard POSIX 1003.1b Functions
for Standardisation of
RTOS and Inter Process Communication Functions, Types of Real
Time Operating Systems
RTOS μ C/OS-II, RTOS Vx Works.

10 Hours

TEXTBOOK

Embedded System Architecture & Programming by Raj Kamal, TMH,
2008 (latest edition).

REFERENCE BOOKS

12. **Introduction to Embedded System Design – A certified Hardware / Software** by Bank Vahid, John Wikey & Sons, 2002.
13. **An embedded Software Primer** by David E Simon, Pearson Edition 1999.

Lab Work:(Part of the theory class)

5. Write C prog to initialise the I/O ports and interface the following:
 - a. LED / LCD Display
 - b. Stepper Motor
 - c. Elevator

- d. Dot – matrix Printer.
6. Write C Prog using ADC/DAC to perform various conversions.
7. Write C Prog for delay using in-built timer.
8. Write C prog for serial-communication using in-built 8251.
9. Write C prog for Scheduling algorithms like FIFO, SJF and Round-Robin
10. Implement Real-Time deadline algorithms.
11. Write C Prog. to control I/O devices (hard disk, speaker, etc).
12. Write C Prog to test the functions of Semaphore, Mutex, Lock etc.
13. Write C Prog to communicate between processes using Pipe, Send() & Recev(), IPC().
14. Write C Prog to perform matrix multiplication using pthreads.

Embedded Systems : Architecture, Programming, and Design,
Raj Kamal, 2nd Edn. TMH, 2008.

REFERENCE BOOKS:

1. **Embedded System Design – A certified Hardware / Software Introduction**, Frank Vahid, John Wikey & Sons, 2002.
2. **An embedded Software Primer** by David E Simon, Pearson Edition 1999.

SPEECH PROCESSING

Subject Code	: 10EC756	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

PRODUCTION AND CLASSIFICATION OF SPEECH SOUNDS:

Introduction, mechanism of speech production. Acoustic phonetics: vowels, diphthongs, semivowels, nasals, fricatives, stops and affricates. **6 Hrs**

UNIT - 2

TIME-DOMAIN METHODS FOR SPEECH PROCESSING: time dependent processing of speech, short-time energy and average magnitude, short-time average zero crossing rate. **6 Hrs**

UNIT - 3

Speech vs. silence detection, pitch period estimation using parallel processing approach, short-time autocorrelation function. **7 Hrs**

UNIT - 4

Brief Applications of temporal processing of speech signals in synthesis, enhancement, hearing applications and clear speech. **7 Hrs**

UNIT - 5

FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING: Introduction, definitions and properties: Fourier transforms interpretation and linear filter interpretation, sampling rates in time and frequency. **7 Hrs**

UNIT - 6

Filter bank summation and overlap add methods for short-time synthesis of speech, sinusoidal and harmonic plus noise method of analysis/synthesis. **6 Hrs**

UNIT - 7

HOMOMORPHIC SPEECH PROCESSING: Introduction, homomorphic system for convolution, the complex cepstrum of speech, homomorphic vocoder. **6 Hrs**

UNIT - 8

APPLICATIONS OF SPEECH PROCESSING: Brief applications of speech processing in voice response systems hearing aid design and recognition systems. **7 Hrs**

TEXT BOOK:

1. **Digital Processing of Speech Signals**, L. R. Rabiner and R. W. Schafer, Pearson Education Asia, 2004.

REFERENCE BOOKS:

15. **Discrete Time Speech Signal Processing**, T. F. Quatieri, Pearson Education Asia, 2004.

16. **Speech and Audio Signal Processing: Processing and Perception of Speech and Music**, B. Gold and N. Morgan, John Wiley India Pvt. Ltd, 2004.

**ELECTIVE-3 (GROUP-C)
PROGRAMMING IN C++**

Subject Code	: 10EC761	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

C++, AN OVERVIEW: Getting started, the C++ program, Preprocessor Directives, The Built-In Array Data Type, Dynamic Memory Allocation and Pointers, An Object – based Design, An Object-Oriented Design, An Exception – based Design, An array. **7 Hrs**

UNIT - 2

THE BASIC LANGUAGE: Literal Constant, Variables, Pointer Type, String Types, const Qualifier, Reference Types, the bool type, Enumeration types, Array types. The vector container type. **6 Hrs**

UNIT - 3

OPERATORS: Arithmetic Operators, Equality, Relational and Logical operators, Assignment operators, Increment and Decrement operator, The conditional Operator, Bitwise operator, bitset operations. Statements: if, switch, for Loop, while, break, goto, continue statements. **7 Hrs**

UNIT - 4

FUNCTIONS: Prototype, Argument passing, Recursion and linear function. **6 Hrs**

UNIT - 5

EXCEPTION HANDLING: Throwing an Exception, Catching an exception, Exception Specification and Exceptions and Design Issues. **7 Hrs**

UNIT - 6

CLASSES: Definition, Class Objects, Class Initialization, Class constructor, The class destructor, Class Object Arrays and Vectors. **7 Hrs**

UNIT - 7

Overload Operators, Operators ++ and --, Operators new and delete.

6 Hrs

UNIT - 8

Multiple Inheritances, public, private & protected inheritance, Class scope under Inheritance.

6 Hrs

TEXT BOOK:

1. **C++ Primer**, S. B. Lippman & J. Lajoie, 3rd Edition, Addison Wesley, 2000.

REFERENCE BOOKS:

1. **C++ Program Design: An Introduction to Programming and Object- Oriented Design**. Cohoon and Davidson, 3rd Edn. TMH publication. 2004.
2. **Object Oriented Programming using C++**, R. Lafore, Galgotia Publications, 2004.

REAL-TIME SYSTEMS

Subject Code	: 10EC762	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION TO REAL-TIME SYSTEMS: Historical background, RTS Definition, Classification of Real-time Systems, Time constraints, Classification of Programs.

6 Hrs

UNIT - 2

CONCEPTS OF COMPUTER CONTROL: Introduction, Sequence Control, Loop control, Supervisory control, Centralised computer control, Distributed system, Human-computer interface, Benefits of computer control systems.

6 Hrs

UNIT - 3

COMPUTER HARDWARE REQUIREMENTS FOR RTS: Introduction, General purpose computer, Single chip microcontroller, Specialized processors, Process-related Interfaces, Data transfer techniques, Communications, Standard Interface. **7 Hrs**

UNIT - 4

LANGUAGES FOR REAL-TIME APPLICATIONS: Introduction, Syntax layout and readability, Declaration and Initialization of Variables and Constants, Modularity and Variables, Compilation, Data types, Control Structure, Exception Handling, Low-level facilities, Co routines, Interrupts and Device handling, Concurrency, Real-time support, Overview of real-time languages. **7 Hrs**

UNIT - 5 & 6

OPERATING SYSTEMS: Introduction, Real-time multi-tasking OS, Scheduling strategies, Priority Structures, Task management, Scheduler and real-time clock interrupt handles, Memory Management, Code sharing, Resource control, Task co-operation and communication, Mutual exclusion, Data transfer, Liveness, Minimum OS kernel, Examples. **14 Hrs**

UNIT - 7

DESIGN OF RTSS – GENERAL INTRODUCTION: Introduction, Specification documentation, Preliminary design, Single-program approach, Foreground/background, Multi-tasking approach, Mutual exclusion, Monitors. **6 Hrs**

UNIT - 8

RTS DEVELOPMENT METHODOLOGIES: Introduction, Yourdon Methodology, Requirement definition for Drying Oven, Ward and Mellor Method, Hatley and Pirbhai Method. **6 Hrs**

TEXT BOOKS:

4. **Real - Time Computer Control- An Introduction**, Stuart Bennet, 2nd Edn. Pearson Education. 2005.

REFERENCE BOOKS:

1. **Real-Time Systems Design and Analysis**, Phillip. A. Laplante, second edition, PHI, 2005.
2. **Real-Time Systems Development**, Rob Williams, Elsevier. 2006.
3. **Embedded Systems**, Raj Kamal, Tata Mc Graw Hill, India, 2005.

IMAGE PROCESSING

Subject Code	: 10EC763	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

DIGITAL IMAGE FUNDAMENTALS: What is Digital Image Processing. fundamental Steps in Digital Image Processing, Components of an Image processing system, elements of Visual Perception. **6 Hrs**

UNIT - 2

Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships between Pixels, Linear and Nonlinear Operations. **6 Hrs**

UNIT - 3

IMAGE TRANSFORMS: Two-dimensional orthogonal & unitary transforms, properties of unitary transforms, two dimensional discrete Fourier transform. **7 Hrs**

UNIT - 4

Discrete cosine transform, sine transform, Hadamard transform, Haar transform, Slant transform, KL transform. **7 Hrs**

UNIT - 5

IMAGE ENHANCEMENT: Image Enhancement in Spatial domain, Some Basic Gray Level Transformations, Histogram Processing, Enhancement Using Arithmetic/Logic Operations. **7 Hrs**

UNIT - 6

Basics of Spatial Filtering Image enhancement in the Frequency Domain filters, Smoothing Frequency Domain filters, Sharpening Frequency Domain filters, homomorphic filtering. **6 Hrs**

UNIT - 7

Model of image degradation/restoration process, noise models, Restoration in the Presence of Noise, Only-Spatial Filtering Periodic Noise Reduction by Frequency Domain Filtering, Linear Position-Invariant Degradations, inverse filtering, minimum mean square error (Weiner) Filtering, **7 Hrs**

UNIT - 8

Color Fundamentals. Color Models, Pseudo color Image Processing., processing basics of full color image processing

6 Hrs

TEXT BOOK:

1. **“Digital Image Processing”**, Rafael C.Gonzalez, Richard E. Woods, etl , TMH , 2nd Edition 2010.

REFERENCE BOOKS:

1. **“Fundamentals of Digital Image Processing”**, Anil K. Jain, Pearson Education, 2001.
2. **“Digital Image Processing and Analysis”**, B. Chanda and D. Dutta Majumdar, PHI, 2003.

RADIO FREQUENCY INTEGRATED CIRCUITS

Subject Code	: 10EC764	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

OVERVIEW OF WIRELESS PRINCIPLES: A brief history of wireless systems, Noncellular wireless applications, Shannon, Modulations & Alphabet Soup, Propagation. **3 Hrs**

PASSIVE RLC NETWORKS: Introduction, Parallel RLC Tank, Series RLC Networks, Other RLC networks, RLC Networks as impedance Transformers. **4 Hrs**

UNIT - 2

CHARACTERISTICS OF PASSIVE IC COMPONENTS: Introduction, Interconnect at radio frequencies: Skin effect, resistors, Capacitors, Inductors, Transformers, Interconnect options at high frequency. **6 Hrs**

UNIT - 3

A REVIEW OF MOS DEVICE PHYSICS: Introduction, A little history, FETs, MOSFET physics, The long – channels approximation, operation in weak inversion (sub threshold), MOS device physics in the short – channel regime, Other effects. **3 Hrs**

DISTRIBUTED SYSTEMS: Introduction, Link between lumped and distributed regimes driving-point impedance of iterated structures, Transmission lines in more detail, Behavior of Finite – length transmission lines, summary of transmission line equations, artificial lines. **4 Hrs**

UNIT - 4

THE SMITH CHART AND S-PARAMETERS: Introduction, The smith chart, S-parameters, Band Width Estimation Techniques, Introduction, The method of open – circuit time constant, The method of short circuit time constant, Risetime, Delay and bandwidth. **6 Hrs**

UNIT - 5

HIGH FREQUENCY AMPLIFIER DESIGN: Introduction, Zeros as bandwidth Enhancers, The shunt –series amplifier, Bandwidth Enhancement with f_T Doublers, Tuned amplifiers, Neutralization and unilateralization, Cascaded amplifiers, AM – PM conversion. **7 Hrs**

UNIT - 6

VOLTAGE REFERENCES AND BIASING: Introduction, Review of diode behavior, Diodes and bipolar transistors in CMOS technology, Supply –independent bias circuits, Bandgap voltage reference, Constant g_m bias. **Noise:** Introduction, Thermal noise, Shot noise, Flicker noise, Popcorn noise, Classical two- port noise theory, Examples of noise calculations, A handy rule of thumb, Typical noise performance. **6 Hrs**

UNIT - 7

LOW NOISE AMPLIFIER DESIGN: Introduction, Derivation of intrinsic MOSFET two-port noise parameters, LNA topologies: Power match versus noise match, Power-constrained noise optimization, Design examples, linearity and large signal performance, Spurious – free Dynamic range. **Mixers:** Introduction, Mixer fundamental, Nonlinear systems as linear mixers. **7 Hrs**

UNIT - 8

Multiplier – based mixers, Sub sampling mixers, Diode ring mixers, RF power amplifiers, Introduction, general considerations, Class A, AB, B and C power amplifier, Class D amplifiers, Class E amplifiers Class F amplifiers, Modulation of power amplifiers, summary of PA characteristics, RF PA design examples, additional design considerations, Design summery. **7 Hrs**

TEXT BOOK:

1. **The design of CMOS radio-frequency integrated circuit**, Thomas H. Lee, 2nd edition Cambridge, 2004.

REFERENCE BOOK:

1. **Design of Analog CMOS integrated circuit**, Behzad Razavi, Tata Mc Graw Hill, 2005.

WAVELET TRANSFORMS

Subject Code	: 10EC765	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

CONTINUOUS WAVELET TRANSFORM: Introduction, C-T wavelets, Definition of CWT, The CWT as a correlation. Constant Q-Factor Filtering Interpolation and time frequency resolution, the CWT as an operator, inverse CWT. **6 Hrs**

UNIT - 2

INTRODUCTION TO DISCRETE WAVELET TRANSFORM AND ORTHOGONAL WAVELET DECOMPOSITION: Introduction. Approximation of vectors in nested linear vector spaces, (i) example of approximating vectors in nested subspaces of a finite dimensional linear vector space, (ii) Example of approximating vectors in nested subspaces of an infinite dimensional linear vector space. Example MRA. (i) Bases for the approximations subspaces and Harr scaling function, (ii) Bases for detail subspaces and Haar wavelet. **7 Hrs**

UNIT - 3

MRA, ORTHO NORMAL WAVELETS AND THEIR RELATIONSHIP TO FILTER BANKS: Introduction, Formal definition of an MRA. Construction of a general orthonormal MRA, (i) scaling function and subspaces, (ii) Implication of dilation equation and orthogonality, a wavelet basis for MRA. (i) Two scale relations for (t), (ii) Basis for the detail subspace (iii) Direct sum decomposition, Digital filtering interpolation (i) Decomposition filters, (ii) reconstruction, the signal. **7 Hrs**

UNIT - 4

EXAMPLES OF WAVELETS: Examples of orthogonal basis generating wavelets, (i) Daubechies D_4 scaling function and wavelet. (ii) band limited wavelets, Interpreting orthonormal MRAs for Discrete time MRA, (iii) Basis functions for DTWT. **6 Hrs**

UNIT - 5

ALTERNATIVE WAVELET REPRESENTATIONS: Introduction, Bi-orthogonal wavelet bases, Filtering relationship for bi-orthogonal filters, Examples of bi-orthogonal scaling functions and wavelets. 2-D wavelets.

6 Hrs

UNIT - 6

Non - separable multidimensional wavelets, wavelet packets. Wavelets Transform and Data Compression: Introduction, transform coding, DTWT for image compression (i) Image compression using DTWT and run-length encoding.

7 Hrs

UNIT - 7

(i) Embedded tree image coding (ii) compression with JPEG audio compression (iii) Audio masking, (iv) Wavelet based audio coding.

6 Hrs

UNIT - 8

CONSTRUCTION OF SIMPLE WAVELETS: Construction of simple wavelets like Harr and DB1. Other Applications of Wavelet Transforms: Introduction, wavelet de-noising, speckle removal, edge detection and object isolation, Image fusions, Object detection by wavelet transforms of projections.

7 Hrs

TEXT BOOK:

6. **Wavelet transforms- Introduction to theory and applications**, Raghuvver M.Rao and Ajit S. Bapardikar, Person Education, 2000.

REFERENCE BOOKS:

3. **Wavelet transforms**, Prasad and Iyengar, John Wiley India Pvt. Ltd, 2007.
4. **Wave-let and filter banks**, Gilbert Strang and Nguyen Wellesley Cambridge press, 1996
5. **Insight into WAVELETS from theory to practice**, K.P. Soman and K.L. Ramchandran, Eastern Economy Edition, 2008

MODELING AND SIMULATION OF DATA NETWORKS

Subject Code	: 10EC766	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT – 1&2

DELAY MODELS IN DATA NETWORKS: Queuing Models, M/M/1, M/M/m, M/M/□, M/M/m/m and other Markov System, M/G/1 System, Networks of Transmission Lines, Time Reversibility, Networks of Queues.

12 Hrs

UNIT – 3&4

MULTI-ACCESS COMMUNICATION: Slotted Multi-access and the Aloha System, Splitting Algorithms, Carrier Sensing, Multi-access Reservations, Packet Radio Networks.

12 Hrs

UNIT – 5&6

ROUTING IN DATA NETWORKS: Introduction, Network Algorithms and Shortest Path Routing, Broadcasting Routing Information: Coping with Link Failures, Flow models, Optimal Routing, and Topological Design, Characterization of Optimal Routing, Feasible Direction Methods for Optimal Routing, Projection Methods for Optimum Routing, Routing in the Codex Network.

14 Hrs

UNIT – 7&8

FLOW CONTROL: Introduction, Window Flow Control, Rate Control Schemes, Overview of Flow Control in Practice, Rate Adjustment Algorithms.

14 Hrs

REFERENCE BOOKS:

1. **"Data Networks"** Dimitri Bertsekas and Robert Gallager, 2nd edition, Prentice Hall of India, 2003.

2. **“High-Speed Networks and Internets”** William Stallings, Pearson Education (Asia) Pte. Ltd, 2004.
3. **“High Performance Communication Networks”** J. Walrand and P. Varaya, 2nd edition, Harcourt India Pvt. Ltd. & Morgan Kaufman, 2000.

VIII SEMESTER

WIRELESS COMMUNICATION

Subject Code	: 10EC81	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Introduction to wireless telecommunication systems and Networks, History and Evolution Different generations of wireless cellular networks 1G, 2g,3G and 4G networks.

6 Hrs

UNIT - 2

Common Cellular System components, Common cellular network components, Hardware and software, views of cellular networks, 3G cellular systems components, Cellular component identification Call establishment.

7 Hrs

UNIT - 3

Wireless network architecture and operation, Cellular concept Cell fundamentals, Capacity expansion techniques, Cellular backbone networks, Mobility management, Radio resources and power management Wireless network security.

7 Hrs

UNIT - 4

GSM and TDMA techniques, GSM system overview, GSM Network and system Architecture, GSM channel concepts, GSM identifiers

6 Hrs

UNIT - 5

GSM system operation, Traffic cases, Cal handoff, Roaming, GSM protocol architecture. TDMA systems.

6 Hrs

UNIT - 6

CDMA technology, CDMA overview, CDMA channel concept CDMA operations.

6 Hrs

UNIT - 7

Wireless Modulation techniques and Hardware, Characteristics of air interface, Path loss models, wireless coding techniques, Digital modulation techniques, OFDM, UWB radio techniques, Diversity techniques, Typical GSM Hardware. **7 Hrs**

UNIT - 8

Introduction to wireless LAN 802.11X technologies, Evolution of Wireless LAN Introduction to 802.15X technologies in PAN Application and architecture Bluetooth Introduction to Broadband wireless MAN, 802.16X technologies. **7 Hrs**

TEXT BOOK:

1. **Wireless Telecom Systems and networks**, Mullet: Thomson Learning 2006.

REFERENCE BOOKS:

1. **Mobile Cellular Telecommunication**, Lee W.C.Y, MGH, 2nd, 2009.
2. **Wireless communication** - D P Agrawal: 2nd Edition Thomson learning 2007.
3. **Fundamentals of Wireless Communication**, David Tse, Pramod Viswanath, Cambridge 2005.
4. S. S. Manvi, M. S. Kakkasageri, **“Wireles and Mobile Network concepts and protocols”**, John Wiley India Pvt. Ltd, 1st edition, 2010.
5. **“Wireless Communication – Principles & Practice”**, T.S. Rappaport, PHI 2001.

DIGITAL SWITCHING SYSTEMS

Subject Code	: 10EC82	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Developments of telecommunications, Network structure, Network services, terminology, Regulation, Standards. Introduction to telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM, PDH and SDH, Transmission performance.

7 Hrs

UNIT - 2

EVOLUTION OF SWITCHING SYSTEMS: Introduction, Message switching, Circuit switching, Functions of switching systems, Distribution systems, Basics of crossbar systems, Electronic switching, Digital switching systems.

6 Hrs

DIGITAL SWITCHING SYSTEMS: Fundamentals : Purpose of analysis, Basic central office linkages, Outside plant versus inside plant, Switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, Digital switching system fundamentals, Building blocks of a digital switching system, Basic call processing.

7 Hrs

UNIT - 3

TELECOMMUNICATIONS TRAFFIC: Introduction, Unit of traffic, Congestion, Traffic measurement, Mathematical model, lost call systems, Queuing systems.

6 Hrs

UNIT - 4

SWITCHING SYSTEMS: Introduction, Single stage networks, Gradings, Link Systems, GOS of Linked systems.

6 Hrs

UNIT - 5

TIME DIVISION SWITCHING: Introduction, space and time switching, Time switching networks, Synchronisation.

6 Hrs

UNIT - 6

SWITCHING SYSTEM SOFTWARE: Introduction, Scope, Basic software architecture, Operating systems, Database Management, Concept of generic program, Software architecture for level 1 control, Software architecture for level 2 control, Software architecture for level 3 control, Digital switching system software classification, Call models, Connect sequence, Software linkages during call, Call features, Feature flow diagram, Feature interaction. **7 hrs**

UNIT - 7

MAINTENANCE OF DIGITAL SWITCHING SYSTEM: Introduction, Scope, Software maintenance, Interface of a typical digital switching system central office, System outage and its impact on digital switching system reliability, Impact of software patches on digital switching system maintainability, Embedded patcher concept, Growth of digital switching system central office, Generic program upgrade, A methodology for proper maintenance of digital switching system, Effect of firmware deployment on digital switching system, Firmware-software coupling, Switching system maintainability metrics, Upgrade process success rate, Number of patches applied per year, Diagnostic resolution rate, Reported critical and major faults corrected, A strategy improving software quality, Program for software process improvement, Software processes improvement, Software processes, Metrics, Defect analysis, Defect analysis. **7 Hrs**

UNIT - 8

A GENERIC DIGITAL SWITCHING SYSTEM MODEL: Introduction, Scope, Hardware architecture, Software architecture, Recovery strategy, Simple call through a digital system, Common characteristics of digital switching systems. Analysis report. Reliability analysis. **6 Hrs**

TEXT BOOKS:

1. **Telecommunication and Switching, Traffic and Networks** - J E Flood: Pearson Education, 2002.
2. **Digital Switching Systems**, Syed R. Ali, TMH Ed 2002.

REFERENCE BOOK:

1. **Digital Telephony** - John C Bellamy: Wiley India India Pvt. Ltd, 3rd Ed, 2008.

ELECTIVE –4 (GROUP D)
DISTRIBUTED SYSTEM

Subject Code	: 10EC831	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

CHARACTERIZATION OF DISTRIBUTED SYSTEMS: Introduction, Examples of distributed systems, Resource sharing and the web, Challenges.

7 Hrs

UNIT - 2

SYSTEM MODELS: Introduction, Architectural models, Fundamental mode.

6 Hrs

UNIT - 3

INTERPROCESS COMMUNICATION: Introduction, The API for the internet protocols, External data representation and marshalling, Client-server communication, Group communication.

7 Hrs

UNIT - 4

DISTRIBUTED OBJECTS AND REMOTE INVOCATION: Introduction, Communication between distributed objects, Remote procedure call, Events and notifications.

6 Hrs

UNIT - 5

SECURITY: Introduction, Overview of security technique cryptographic algorithms, Digital signature, Cryptography pragmatics.

7 Hrs

UNIT - 6

TIME & GLOBAL STATES: Introduction, Clocks, Events, Process states, Synchronizing physical clocks, Global states, Distributed debugging.

7 Hrs

UNIT - 7

COORDINATION AND AGREEMENT: Distributed mutual exclusion, Elections, Multicast communication.

6 Hrs

UNIT - 8

CORBA CASE STUDY: Introduction, CORBA RMI, CORBA Services.

6 Hrs

TEXT BOOK:

5. **“Distributed Systems, Concepts & Design”**, George Coulouris, Jean Dollimore, Tim Kindberg, fourth edition, 2006. Pearson education.

REFERENCE BOOK:

7. **“Distributed System Architecture, a Middleware Approach”** Arno puder, Kay Romer, Frank Pilhofer, Morgan Kaufmann publishers.

NETWORK SECURITY

Subject Code	: 10EC832	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

Services, mechanisms and attacks, The OSI security architecture, A model for network security.

6 Hrs

UNIT - 2

SYMMETRIC CIPHERS: Symmetric Cipher Model, Substitution Techniques, Transposition Techniques, Simplified DES, Data encryption standard (DES), The strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of Operation, Evaluation Criteria for Advanced Encryption Standard, The AES Cipher.

7 Hrs

UNIT - 3

Principles of Public-Key Cryptasystems, The RSA algorithm, Key Management, Diffie - Hellman Key Exchange, Elliptic Curve Arithmetic, Authentication functions, Hash Functions. **6 Hrs**

UNIT - 4

Digital signatures, Authentication Protocols, Digital Signature Standard. **7 Hrs**

UNIT - 5

Web Security Consideration, Security socket layer (SSL) and Transport layer security, Secure Electronic Transaction. **6 Hrs**

UNIT - 6

Intruders, Intrusion Detection, Password Management. **6 Hrs**

UNIT - 7

MALICIOUS SOFTWARE: Viruses and Related Threats, Virus Countermeasures. **7 Hrs**

UNIT - 8

Firewalls Design Principles, Trusted Systems. **6 Hrs**

TEXT BOOK:

1. **Cryptography and Network Security**, William Stalling, Pearson Education, 2003.

REFERENCE BOOKS:

1. **Cryptography and Network Security**, Behrouz A. Forouzan, TMH, 2007.
2. **Cryptography and Network Security**, Atul Kahate, TMH, 2003.

OPTICAL NETWORKS

Subject Code	: 10EC833	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION TO OPTICAL NETWORKS: Telecommunication networks, First generation optical networks, Multiplexing techniques, Second generation optical networks, System and network evolution. Non linear effects SPM, CPM, four wave mixing, Solitons. **7 Hrs**

UNIT - 2

COMPONENTS: Couplers, isolators and Circulators, Multiplexes and filters Optical amplifiers. **6 Hrs**

UNIT - 3

Transmitters, detectors, Switches, Wavelength converters. **6 Hrs**

UNIT - 4

TRANSMISSION SYSTEM ENGINEERING: System model, Power penalty, Transmitter, receiver, optical amplifiers, Crosstalk, Dispersion, Overall design Consideration. **7 Hrs**

UNIT - 5

FIRST GENERATION NETWORKS: SONET/SDH, Computer interconnects, Mans, Layered architecture for SONET and second generation networks. **6 Hrs**

UNIT - 6

WAVELENGTH ROUTING NETWORKS: Optical layer, Node design, Network design and operation, routing and wavelength assignment architectural variations. **6 Hrs**

UNIT - 7

VIRTUAL TOPOLOGY DESIGN: Virtual topology design problem, Combines SONET/WDM network design, an ILP formulation, Regular virtual topologies, Control and management, Network management configuration management, Performance management, fault management.

7 Hrs

UNIT - 8

ACCESS NETWORKS: Network architecture overview, present and future access networks, HFC, FTTC, Optical access networks Deployment considerations, Photonic packet switching, OTDM, Multiplexing and demultiplexing Synchronisation.

7 Hrs

TEXT BOOK:

3. **Optical networks: A practical perspective** Kumar Sivarajan and Rajiv Ramaswamy: Morgan Kauffman 1998.

REFERENCE BOOKS:

14. **Optical Communication Networks:** Biswajit Mukherjee: TMG 1998.
15. **Optical Networks,** Ulysees Black: Pearson education 2007.

HIGH PERFORMANCE COMPUTER NETWORKS

Subject Code	: 10EC834	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

History of Communication Networks, Networking principles, Future networks Internet, Pure TAM Network, Cable Network, Wireless.

6 Hrs

UNIT - 2

NETWORK SERVICES AND LAYERED ARCHITECTURE: Applications, Traffic characterization and quality of services, Network

services, High performance networks, Network Elements., Layered applications, Open data network model, Network architectures, Network bottlenecks. **7 Hrs**

UNIT - 3

INTERNET AND TCP/IP NETWORKS: Multicast IP, Mobile IP, TCP and UDP, Applications, FTP, SMTP. Internet success and limitations, Performance of TCP/IP Networks, Performance of circuit switched networks. **7 Hrs**

UNIT - 4

SONET, DWDM, FTH, DSL, Intelligent networks CATV. **6 Hrs**

UNIT - 5

ATM: Main features of ATM, Addressing, signaling and Routing, ATM header structure, ATM AAL, Internetworking with ATM. **6 Hrs**

UNIT - 6

WIRELESS NETWORKS: Link level design, Channel Access, Network design, Wireless networks today, Future networks, ad hoc networks, High speed Digital cellular, Home RF and Bluetooth. **7 Hrs**

UNIT - 7

Control of networks, Objectives and methods of control, Circuit switched networks, Datagram Networks Network economics, Derived demand for network services, ISPs, subscriber demand model, Empirical model. **7 Hrs**

UNIT - 8

OPTICAL NETWORKS: WDM systems, Optical cross connects, Optical LANs, Optical paths and networks. **6 Hrs**

TEXT BOOK:

5. **High Performance Communication Networks**, Warland and Varaiya: Morgan Kauffman/ Elsvier 2nd Edition 2000.

REFERENCE BOOKS:

1. **High-Speed Networks and Internet: Performance and Quality of service**, William Stallings, Pearson Edu., 2001.
2. **Building High-Speed Networks**, Tere Parnell, TMGH, 2000.

INTERNET ENGINEERING

Subject Code	: 10EC835	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

INTRODUCTION: Communication model, Communication software, and communication protocol: Representation, Development methods, Protocol engineering process. **NETWORK REFERENCE MODEL:** Layered architecture, Network services and interfaces, protocol functions, OSI model, TCP/IP protocol suite, Application protocols. **7 Hrs**

UNIT - 2

PROTOCOL SPECIFICATION: Communication service specification, Protocol entity specification, Interface specifications, Interactions, Multimedia protocol specifications, Internet protocol specifications. **6 Hrs**

UNIT - 3

SPECIFICATION AND DESCRIPTION LANGUAGE (SDL): A protocol specification language: SDL. **6 Hrs**

UNIT - 4

Examples of SDL based protocol specifications, Other protocol specification languages. Protocol Verification And Validation, Protocol verification, Verification of a protocol using finite state machines. **7 Hrs**

UNIT - 5

Protocol validation, Protocol design errors, and protocol validation approaches, SDL based protocol verification, SDL based protocol validation. **6 Hrs**

UNIT - 6

PROTOCOL CONFORMANCE TESTING: Conformance testing methodology and framework, Conformance test architectures, Test sequence generation methods, Distribute architecture by local methods, Conformance testing with TTCN, Conformance testing of RIP, Multimedia applications testing, SDL based tools for conformance testing. **7 Hrs**

UNIT - 7

PROTOCOL PERFORMANCE TESTING: SDL based performance testing of TCP, OSPF, Interoperability testing, SDL based interoperability testing of CSMA/CD and CSMA/CA protocol using bridge, Scalability testing. **7 Hrs**

UNIT - 8

PROTOCOL SYNTHESIS: Synthesis methods, interactive synthesis algorithms, automatic synthesis algorithm, automatic synthesis of SDL from MSC protocol re synthesis. **6 Hrs**

TEXT BOOK:

3. **Communication Protocol Engineering**, P. Venkatarm and S. S. Manvi, PHI, 2004.

REFERENCES BOOKS:

1. **The Internet and its Protocols**, Adrian Farrel, Elsevier, 2006.
2. **TCP/IP Protocol Stack**, B A Forouzan, TMH, 2006.

ELECTIVE –5 (GROUP E)

MULTIMEDIA COMMUNICATIONS

Subject Code	: 10EC841	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

MULTIMEDIA COMMUNICATIONS: Introduction, multimedia information representation, multimedia networks, multimedia applications,

media types, communication modes, network types, multipoint conferencing, network QoS application QoS. **6 Hrs**

UNIT - 2

MULTIMEDIA INFORMATION REPRESENTATION: Introduction, digital principles, text, images, audio, video. **7 Hrs**

UNIT - 3

TEXT AND IMAGE COMPRESSION: Introduction, compression principles, text compression, image compression. **6 Hrs**

UNIT - 4

AUDIO AND VIDEO COMPRESSION: Introduction, audio compression, DPCM, ADPCM, APC, LPC, video compression, video compression principles, H.261, H.263, MPEG, MPEG-1, MPEG-2, and MPEG-4. **7 Hrs**

UNIT - 5

MULTIMEDIA INFORMATION NETWORKS: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI High-speed LANs, LAN protocol. **6 Hrs**

UNIT - 6

THE INTERNET: Introduction, IP Datagrams, Fragmentation, IP Address, ARP and RARP, QoS Support, IPv8. **7 Hrs**

UNIT - 7

BROADBAND ATM NETWORKS: Introduction, Cell format, Switch and Protocol Architecture ATM LANs. **6 Hrs**

UNIT - 8

TRANSPORT PROTOCOL: Introduction, TCP/IP, TCP, UDP, RTP and RTCP. **7 Hrs**

TEXT BOOK:

1. **Multimedia Communications: Applications, Networks, Protocols and Standards**, Fred Halsall, Pearson Education, Asia, Second Indian reprint 2002.

REFERENCE BOOKS:

1. **Multimedia Information Networking**, Nalin K. Sharda, PHI, 2003.
2. **“Multimedia Fundamentals: Vol 1 - Media Coding and Content Processing”**, Ralf Steinmetz, Klara Narstedt, Pearson Education, 2004.
3. **“Multimedia Systems Design”**, Prabhat K. Andleigh, Kiran Thakrar, PHI, 2004.

REAL TIME OPERATING SYSTEMS

Subject Code	: 10EC842	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT 1

Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems. **6 Hrs**

UNIT 2

System Resources: Resource Analysis, Real-Time Service Utility, Scheduling Classes, The Cyclic Executive, Scheduler Concepts, Preemptive Fixed Priority Scheduling Policies, Real-Time OS, Thread Safe Reentrant Functions. **7 Hrs**

UNIT 3

Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies. **6 Hrs**

UNIT 4

I/O Resources:

Worst-case Execution time, Intermediate I/O, Execution efficiency, I/O Architecture.

Memory:

Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash filesystems. **7 Hrs**

UNIT 5

Multiresource Services:

Blocking, Deadlock and livelock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services:

Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services. **7 Hrs**

UNIT 6

Embedded System Components:

Firmware components, RTOS system software mechanisms, Software application components.

Debugging Components:

Exceptions assert, Checking return codes, Single-step debugging, kernel scheduler traces, Test access ports, Trace ports, Power-On self test and diagnostics, External test equipment, Application-level debugging.

7 Hrs

UNIT 7

Performance Tuning:

Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and Call frequency, Fundamental optimizations.

6 Hrs

UNIT 8

High availability and Reliability Design:

Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design trade offs, Hierarchical applications for Fail-safe design.

Design of RTOS – PIC microcontroller. (Chap 13 of book Myke Predko)

7 Hrs

References:

1. **“Real-Time Embedded Systems and Components”**, Sam Siewert, Cengage Learning India Edition, 2007.
2. **“Programming and Customizing the PIC microcontroller”**, Myke Predko, 3rd Ed, TMH, 2008

GSM

Subject Code	: 10EC843	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

GSM ARCHITECTURE AND INTERFACES: Introduction, GSM frequency bands, GSM PLMN, Objectives of a GSM PLMN, GSM PLMN Services, GSM Subsystems, GSM Subsystems entities, GSM interfaces, The radio interface (MS to BSC), A_{bits} interface (BTS to BSC), A interface (BSC to MSC), Interfaces between other GSM entities, Mapping of GSM layers onto OSI layers. **6 Hrs**

UNIT - 2

RADIO LINK FEATURES IN GSM SYSTEMS: Introduction, Radio link measurements, Radio link features of GSM, Dynamic power control, Discontinuous transmission (DTX), SFH, Future techniques to reduce interface in GSM, Channel borrowing, Smart antenna. **7 Hrs**

UNIT - 3

GSM LOGICAL CHANNELS AND FRAME STRUCTURE: Introduction, GSM logical channels, Allowed logical channel combinations, TCH multi frame for TCH/H, CCH multi frame, GSM frame structure, GSM bursts, Normal burst, Synchronization burst, Frequency correction channel burst, Access burst, Data encryption in GSM, Mobility management, Location registration, Mobile identification. **7 Hrs**

UNIT - 4

SPEECH CODING IN GSM: Introduction, Speech coding methods, Speech code attributes, Transmission bit rate, Delay, Complexity, Quality, LPAS, ITU-T standards, Bit rate, Waveform coding, Time domain waveform coding, Frequency domain waveform coding, Vocoders, Full-rate vocoder, Half-rate vocoder. **MESSAGES, SERVICES, AND CALL FLOWS IN GSM:** Introduction, GSM PLMN services. **7 Hrs**

UNIT - 5

GSM messages, MS-BS interface, BS to MSC messages on the A interface, MSC to VLR and HLR, GSM call setup by an MS, Mobile-Terminated call, Call release, Handover. Data services, Introduction, Data interworking, GSM data services, Interconnection for switched data, Group 3 fax, Packet data on the signaling channel, User-to-user signaling, SMS, GSM GPRS.

6 Hrs

UNIT - 6

PRIVACY AND SECURITY IN GSM: Introduction, Wireless security requirements, Privacy of communications, Authentication requirements, System lifetime requirements, Physical requirements, SIM cards, Security algorithms for GSM, Token-based authentication, Token-based registration, Token-based challenge.

6 Hrs

UNIT - 7

PLANNING AND DESIGN OF A GSM WIRELESS NETWORK: Introduction, Tele traffic models, Call model, Topology model, Mobility in cellular / PCS networks, Application of a fluid flow model, Planning of a wireless network, Radio design for a cellular / PCS network, Radio link design, Coverage planning, Design of a wireless system, Service requirements, Constraints for hardware implementation, Propagation path loss, System requirements, Spectral efficiency of a wireless system, Receiver sensitivity and link budget, Selection of modulation scheme, Design of TDMA frame, Relationship between delay spread and symbol rate, Design example for a GSM system.

7 Hrs

UNIT - 8

MANAGEMENT OF GSM NETWORKS: Introduction, Traditional approaches to NM, TMN, TMN layers, TMN nodes, TMN interface, TMN management services, Management requirements for wireless networks, Management of radio resources, Personal mobility management, Terminal mobility, Service mobility management, Platform-centered management, SNMP, OSI systems management, NM interface and functionality, NMS functionality, OMC functionality, Management of GSM network, TMN applications, GSM information model, GSM containment tree, Future work items.

7 Hrs

TEXT BOOK:

1. **“Principles of Applications of GSM”**, Vijay K. Garg & Joseph E. Wilkes, Pearson education/ PHI, 1999.

REFERENCE BOOKS:

1. **GSM: Evolution towards 3rd Generation Systems**, (Editor), Z. Zvonar Peter Jung, Karl Kammerlander Springer; 1st edition 1998
2. **GSM & UMTS: The Creation of Global Mobile Communication**, **Friedhelm Hillebrand**, John Wiley & Sons; 2001.

ADHOC WIRELESS NETWORKS

Subject Code	: 10EC844	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

AD HOC NETWORKS: Introduction, Issues in Ad hoc wireless networks, Ad hoc wireless internet. **6 Hrs**

UNIT - 2

MAC PROTOCOLS FOR AD HOC WIRELESS NETWORKS: Introduction, Issues in designing a MAC protocol for Ad hoc wireless Networks, Design goals of a MAC protocol for Ad hoc wireless Networks, Classification of MAC protocols. **7 Hrs**

UNIT - 3

Contention - based MAC protocols with scheduling mechanism, MAC protocols that use directional antennas, Other MAC protocols. **6 Hrs**

UNIT - 4

ROUTING PROTOCOLS FOR AD HOC WIRELESS NETWORKS: Introduction, Issues in designing a routing protocol for Ad hoc wireless Networks, Classification of routing protocols, Table drive routing protocol, On-demand routing protocol. **7 Hrs**

UNIT - 5

Hybrid routing protocol, Routing protocols with effective flooding mechanisms, Hierarchical routing protocols, Power aware routing protocols.

6 Hrs

UNIT - 6**TRANSPORT LAYER PROTOCOLS FOR AD HOC WIRELESS**

NETWORKS: Introduction, Issues in designing a transport layer protocol for Ad hoc wireless Networks, Design goals of a transport layer protocol for Ad hoc wireless Networks.

7 Hrs

UNIT - 7

SECURITY: Security in wireless Ad hoc wireless Networks, Network security requirements, Issues & challenges in security provisioning.

6 Hrs

UNIT - 8**QUALITY OF SERVICE IN AD HOC WIRELESS NETWORKS:**

Introduction, Issues and challenges in providing QoS in Ad hoc wireless Networks, Classification of QoS solutions.

7 Hrs

TEXT BOOK:

3. “Ad hoc wireless Networks”, C. Siva Ram Murthy & B. S. Manoj, Pearson Education, 2nd Edition, reprint 2005.

REFERENCE BOOKS:

1. “Ad hoc wireless Networks”, Ozan K. Tonguz and Gianguigi Ferrari, Wiley
2. “Ad hoc wireless Networking”, Xiuzhen Cheng, Xiao Hung, Ding-Zhu Du, Kluwer Academic publishers.

OPTICAL COMPUTING

Subject Code	: 10EC845	IA Marks	: 25
No. of Lecture Hrs/Week	: 04	Exam Hours	: 03
Total no. of Lecture Hrs.	: 52	Exam Marks	: 100

UNIT - 1

MATHEMATICAL AND DIGITAL IMAGE FUNDAMENTALS:

Introduction, Fourier Transform, discrete Fourier transform, basic diffraction theory, Fourier transform property of lens, sampling and quantization, image enhancement, image restoration.

7 Hrs

UNIT - 2

LINER OPTICAL PROCESSING: Introduction, photographic film, spatial filtering using binary filters, holography, inverse filtering, Deblurring.

6 Hrs

UNIT - 3

ANALOG OPTICAL ARITHMETIC: Introduction, Halftone processing, nonlinear optical processing, Arithmetic operations.

6 Hrs

UNIT - 4

RECOGNITION USING ANALOG OPTICAL SYSTEMS: Introduction, Matched filter, Joint transform correlation, Phase-only filter, Amplitude modulated recognition filters, Generalized correlation filter, Mellin transform based correlation.

7 Hrs

UNIT - 5

DIGITAL OPTICAL COMPUTING DEVICES: Introduction, Nonlinear devices, Integrated optics, Threshold devices, Spatial high modulators, Theta modulation devices.

6 Hrs

UNIT - 6

SHADOW-CASTING AND SYMBOLIC SUBSTITUTION: Introduction, Shadow casting system and design algorithm, POSC logic operations, POSC multiprocessor, Parallel ALU using POSC, Sequential ALU using POSC, POSC image processing, Symbolic substitutions, Optical implementation of symbolic substitution, Limitations and challenges.

7 Hrs

UNIT - 7

OPTICAL MATRIX PROCESSING: Introduction, Multiplication, Multiplication using convolution, Matrix operations, Cellular logic architecture, Programmable logic array. **6 Hrs**

UNIT - 8

ARTIFICIAL INTELLIGENT COMPUTATIONS: Introduction, Neural networks, Associative memory, Optical implementations, Interconnections, Artificial Intelligence. **7 Hrs**

TEXT BOOK:

2. **“Optical Computing An Introduction”**, Mohammed A. Karim, John Wiley & Sons, 1992.

REFERENCE BOOKS:

1. **Optical Signal Processing** by Vanderlugt John willy & sons NY 1992.
2. **Signal Processing in Optics** - Bradly G Boore Oxford University Press 1998.