	Sri Venkateshwara College of Engineering Vidyanagar, Bengaluru - 562157 Minutes of Meeting Register	Format No.	ACD44
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Meeting No. SVCE/DECE-FDP/2015-16/01 Date: 14.07.2015

Members Present:

Sl. No.	Name of the faculty	Signature with date	Sl. No.	Name of the faculty	Signature with date
1	Dr.SSN		16	ASR	
2	GRP		17	MKS	
3	SKS		18	NTN	
4	RPP		19	MHI	
5	SKN		20	RAK	
6	JJJ				
7	MSP				
8	DRB				
9	PSR				
10	RNG				
11	PMV				
12	SRT				
13	AGB				
14	SSR				
15	ANS				

14/7/15

Programme Coordinator

Action Plan for this Meeting

Sl No	Action Plan	Responsibility
1	Workshop on "Design and implementation of Real Time Applications using VLSI"	All Staff
2	Participation details	All Staff
3	Arrangements	All Staff
4	Any other issues	All Staff

14/01/15

Meeting Chair

Note: C – Completed, IP – In Progress, NS – Not Started

Workshop on "Design and implementation of Real time applications using VLSI"

This design cycle is normally represented as a step as shown in below

1. System specification
2. Functional design
3. Logic design
4. Circuit design
5. Physical design
6. Fabrication
7. Packaging of System specification

The specification of the system to be designed exactly specified in this step. It considers performance, functionality and the physical dimensions of the design of Functional design: In this step, behavioural aspects of the system and considered. The outcome is usually a timing diagram or other relationship o Logic design: In this step, the functional design is converted into a logic design, using the Boolean. These expressions are minimizing to achieve the smallest logic design o Circuit design: The step involves conversion of boolean expression into a circuit representation by taking into consideration of speed and power of Physical design: In this step, the circuit representation of each component is converted a geometric representation of Design verification: In this step, the layout is verified to ensure the layout meets the system specification and fabrication requirements ofs Fabrication: This step is followed design verification the fabrication power consists of several steps like preparation of wafer, deposition.

The workshop intends to provide opportunities to faculty member, research scholar, technical assistant as-well-as students to enrich their intellectual validity and further their professional growth. The major focus of the workshop is for the upgradation of outcome based teaching & learning skills and research for the participants in the field of Micro & Nano electronic devices and also for VLSI design in nanoscale using advanced simulation tools. Hands-on exposure to

Modern VLSI design and analysis tools like Cadence Virtuoso, Visual TCAD, TSPICE will also be offered to blend the research with implementation for real life problem. Moreover this workshop aims to inculcate learning values in students and monitoring their progress in career.